A 10-Gb/s, -32.6dBm Receiver with 3.5Gbps APD for XGPON/XGSPON Mass Production

Rui Wang, Xin Zhao, Yingfan Ling, Gaoyong Fan, Zhijun Cai and Rui Tao

Chengdu Meenyi Electronic Technology Co.,Ltd, Chengdu, China

wangrui@meenyi.com

Abstract: A 10-Gb/s low-power low-noise optical receiver in 65nm CMOS is presented and can achieve a sensitivity of -32.6dBm after pairing with a 3.5Gbps low-cost APD, which provides a solution necessary for mass production of XGPON/XGSPON. © 2021 The Author(s)

1. Introduction

As the Electrical-to-Optical paradigm shift has happened in the consumer access networks, there are high demands for 10Gbps Passive Optical Network (XGPON/XGSPON) using mature CMOS technology, which is the industrialization upgrading from 2.5Gbps PON (GPON) [1]. With the data rate increasing from 2.5Gbps to 10Gbps, the bandwidth of both APD and transimpendance amplifier (TIA) of the optical receiver has to be increased accordingly. Although it is relatively easier to boost performance of the TIA using either different circuit designs or more advanced deep-submicron technology, boosting bandwidth of the avalanche photodiode (APD) is much more costly since most of the cost in the optical receiver comes from cost of APD itself. As a result, implementing low-cost APD with high performance TIA provides low-cost transistor-outline controller-area-network (TO-can) solution necessary for the mass production of XGPON/XGSPON. However, lower bandwidth APD severely reduces the root-mean-square (rms) current injected into TIA while low-cost APD also brings more capacitance loading at the TIA input, both of which will cause power penalty resulting in lower sensitivity for the receiver. At the same time, although continuous-time linear equalizer (CTLE) can be used to boost the bandwidth to compensate for sensitivity drop, more noise will be introduced while phase-margin will become even worse, both of which will limit the sensitivity improvement [2]. Therefore, a new low-noise, high-bandwidth receiver design is required to compensate for the Opto-Electronics (OE) bandwidth drop with the implementation of low-cost APD in the upcoming mass production of XGPON/XGSPON.

2. 10-Gb/s Low-Power, High-Bandwidth, Low-Noise Optical Receiver

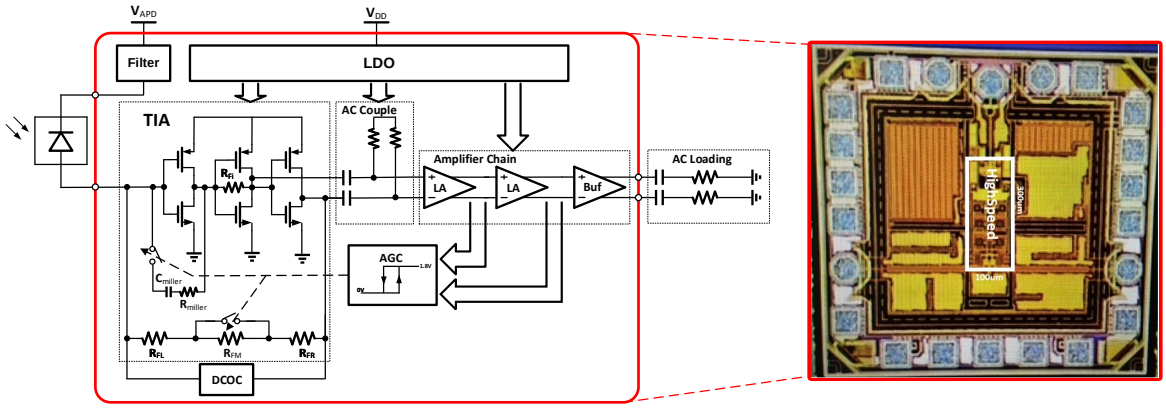

Fig. 1. 10-Gb/s Optical Receiver Architecture and its Chip Photo

2.1. Receiver Design Overview

Fig. 1 shows the block diagram of our proposed low-power, high-bandwidth, low-noise optical receiver design, which includes a 3.5Gbps low-cost APD, a TIA with direct current offset correction (DCOC) and discrete auto-

matic gain control (AGC), a low-dropout regulator (LDO), a low-pass filter with high-voltage capacitors and a limiting amplifiers (LAs) chain.

Unlike traditional receiver design, where bandwidth of the APD is the same or even larger than data rate of receiver itself, bandwidth of the APD in our proposed receiver architecture is smaller than half of the data rate and it prompts the following four design optimizations. First, bandwidth of our proposed TIA has to be larger than 10GHz without capacitive loading at the front. Due to the low bandwidth and large capacitive loading from low-cost APD, bandwidth of the TIA has to be over-designed so that it won't fall below one third of the bandwidth where inter-symbol interference (ISI) will introduce extra group delay apart from the usual power penalty. Second, discrete AGC is more optimized to achieve the bandwidth required by our proposed TIA in terms of power consumption. Third, continuous-time linear equalizer (CTLE) is eliminated and replaced by a lower-power limiting amplifier in our receiver design. The saved power is re-diverted into the TIA to boost bandwidth while keeping noise relatively low. Four, our proposed TIA structure increases trans-impedance of TIA while keeping its input impedance the same as traditional design to avoid reducing input overload current [3]. The increased trans-impedance relaxes the gain requirement of the amplifier chain so that only three LAs are implemented unlike traditional CTLA + three LAs combo, which further increases bandwidth of the receiver with even lower power consumption.

2.2. *High-Bandwidth, Low-noise Pseudo-balanced TIA Design*

The proposed TIA design consists of a high-gain high-bandwidth amplifier and its feedback resistors to form a shunt-shunt feedback architecture. A DCOC loop is connected between TIA input/output so that the voltage between these two nodes are locked into the same voltage even with large current input. In order to increase the dynamic range, a discrete AGC is used to switch our proposed TIA between low-gain mode and high-gain mode. In the high-gain mode, the feedback resistor is the sum of R_{FL}, R_{FR} and R_{FM} while R_{FM} is shorted in low-gain mode. According to feedback theory, when both open-loop gain and its poles/zeros are fixed, smaller feedback resistor results in larger bandwidth and can thus worsen the group-delay of the TIA. Our proposed structure, however, solves the aforementioned problem by introducing miller compensation between the input/output of first inverter to push the main pole towards lower frequency, which is comprised of C_{miller} and R_{miller}. Also, using miller compensation can reduce the required capacitance of C_{miller} and R_{miller} is implemented to alleviate the feed-forward due to this compensation.

Our proposed high-gain high-bandwidth amplifier is comprised of three CMOS inverters in series and the second one forms another TIA with its local shunt-shunt feedback resistor R_{Fi}. The three CMOS-inverter in series structure is more power-efficient since it can naturally provide differential signals without introducing a dummy TIA. Also, with the same f_T, CMOS inverter is able to achieve similar noise and bandwidth performance with one third of the size and current comparing to its nMOSFET counterpart [4]. The functionalities of the feedback resistor R_{Fi} are two folds. First, gain of the first two inverters can be approximated to $(g_{mn}+g_{mp})*R_{Fi}$. By choosing metal resistor instead of poly, R_{Fi} can be made relatively constant under different corner conditions so that both the TIA gain and bandwidth won't vary due to the open-loop gain. Second, R_{Fi} pushes the output poles of first two inverters' to higher frequency so that the proposed open-loop gain amplifier can be approximated to a two-pole system for better phase-margin.

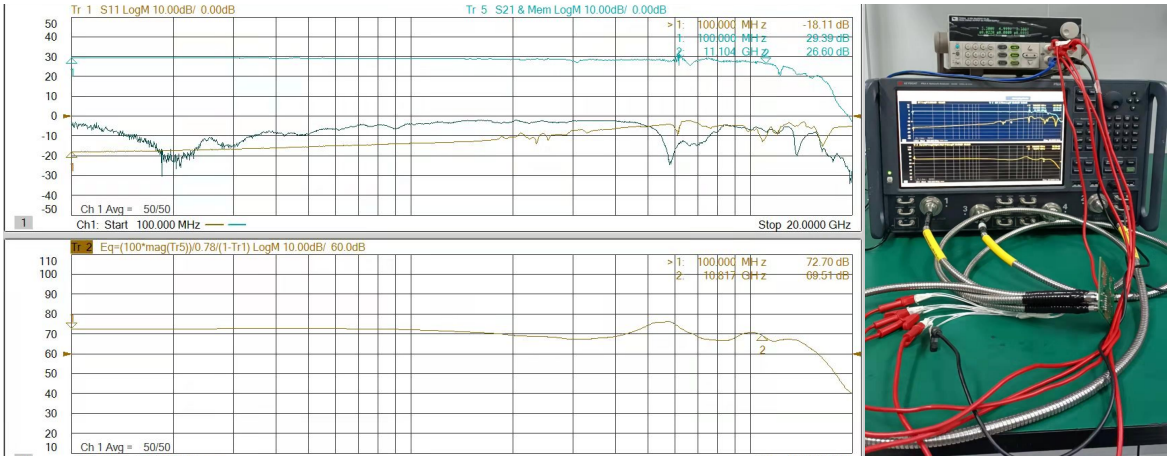

Fig. 2. S-Parameter Testing Result and its Testing Setup

3. Receiver with 3.5Gbps APD Testing Results

The proposed receiver is implemented in 65nm CMOS technology and its chip layout can be seen in Fig. 1 with high-speed path occupying an area of $0.1\text{x}0.3mm^2$. The whole receiver consumes 26.4mA under 3.3V power supply. Without APD, we have tested the s-parameter of our receiver with both results and testing setup shown in Fig. 2. By injecting power of -40dBm through AC-coupling, our receiver is working in high-gain mode and has a gain of 72.7dB with a bandwidth of 10.82GHz.

Through wire-bonding our receiver to a low-cost 3.5Gbps APD, we have tested both sensitivity and output eye-diagram of our receiver. Using 10-Gb/s PRBS31 pattern input, our proposed receiver is able to achieve a sensitivity of -32.6dBm with the bit-error-rate (BER) of 10^{-3} and a sensitivity of -27dBm with the BER of 10^{-12}. Using 2.5-Gb/s PRBS23 pattern input, sensitivity of our proposed receiver can reach -39.2dBm with the BER of 10^{-3}. Under 2.5-Gb/s data rate, noise is the only limitation for the sensitivity of our receiver. Thus, the input referred noise of our receiver can be derived since our test shows that rms current input of the receiver is 11.3uA with -30dBm optical power injected into the APD. Therefore, the input referred noise of our receiver including that of APD results in as low as 440nArms.

The resulting eye-diagram of our receiver with 10-Gb/s PRBS31 pattern input can be seen in Fig. 3. The left figure shows our receiver output eye-diagram with input optical power of -26dBm, which is close to our receiver sensitivity. The right figure presents the eye-diagram when our receiver is working close to overload condition since optical input power of -5dBm corresponds to the rms current input of receiver at 1.7mA. Although there are limited amount of distortion due to operating close to overload condition, the final BER won't be affected since receiver BER is smaller than 10^{-12} once optical power input of our receiver is larger than -27dBm.

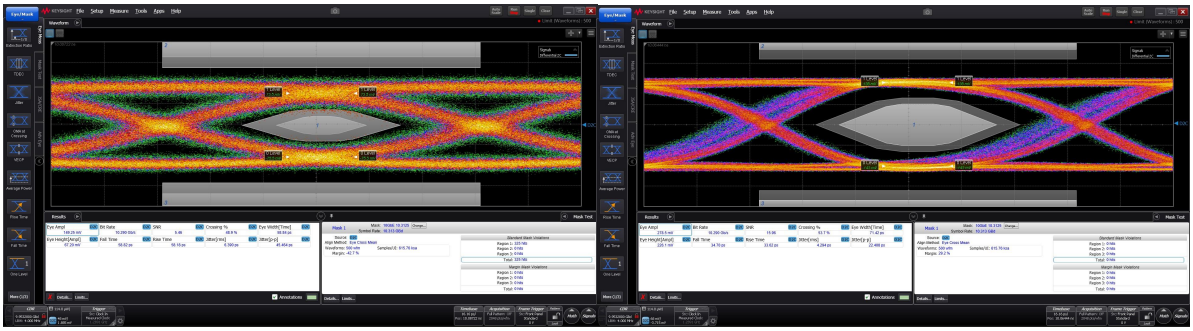

Fig. 3. 10-Gb/s Eye-Diagram of the Receiver Differential Output when Receiver Input Optical Power is at -26dBm (Left) and at -5dBm (Right) respectively

4. Conclusions

A 10-Gb/s low-power low-noise optical receiver in 65nm CMOS is presented and it can achieve a sensitivity of -32.6dBm after pairing with a 3.5Gbps low-cost APD. By implementing our proposed pseudo-differential TIA design as well as reconstructing the receiver architecture itself, both low-noise and high-bandwidth requirements can be fulfilled simultaneously while maintaining low power consumption. Therefore, our proposed low-noise, high-bandwidth receiver design pairing with low-cost APD is able to provide a low-cost TO-can solution for the upcoming mass production of XGPON/XGSPON.

References

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