Streamlined Architecture for Thermal Control and Stabilization of Cascaded DWDM Micro-Ring Filters Bus

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Abstract: We demonstrate the thermal control of cascaded micro-ring DWDM filters using a single photodiode. The streamlined implementation maintains stable operation of the 8-ring bus with less than 0.1dB BER power penalty on an 8x10Gb/s link. © 2022 The Author(s)

1. Introduction

Micro-ring resonators (MRRs) are a key component in building dense multi-Terabit per second DWDM photonic interconnects [1]. Their small footprint and wavelength selectivity allows for compact DWDM demux at the receivers of these interconnects. Using multiple photodiodes to observe individual rings limits the achievable bandwidth density as the electrical connections are often larger than the MRRs themselves, while single monitor solutions require execution of a search algorithm with every thermal disturbance [2, 3]. This work demonstrates the first multi-channel implementation of a thermal dithering control scheme using a single photodiode streamlined architecture. The digital system implementation maintains stable operation of the 8-ring bus under >20°C temperature variations with negligible bit error rate (BER) power penalty of less than 0.1dB for the 8x10Gb/s link.

2. System Architecture

An overview of the implemented thermal control system is shown in Fig. 1. At the core is a photonic integrated circuit (PIC) with eight cascaded micro-ring filters. Light is launched into the bus waveguide and each ring can pick a wavelength off the bus and couple it into an output waveguide. All remaining light is fed into a Thorlabs PDA10CS photo detector and transimpedance amplifier. To generate optical PRBS31 streams and measure BER, a HiTechGlobal HTG-930 FPGA and eight 10Gb/s 80km DWDM SFP+ modules are used. The optical signals are muxed together by a commercially available DWDM mux, then demuxed by the PIC, and finally looped back to the SFP+ modules. The VOA is used to measure the BER at different input power levels to the SFP+ modules. The

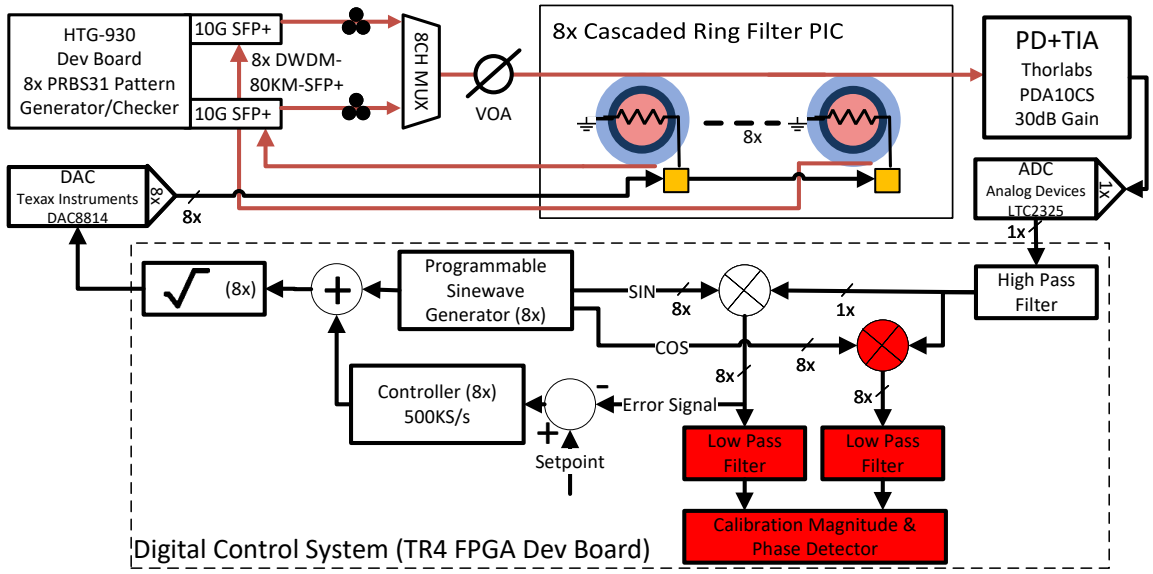

Fig. 1: Schematic representation of implemented system. Red and black lines indicate optical and electrical connections, respectively. Red blocks are used for system calibration.

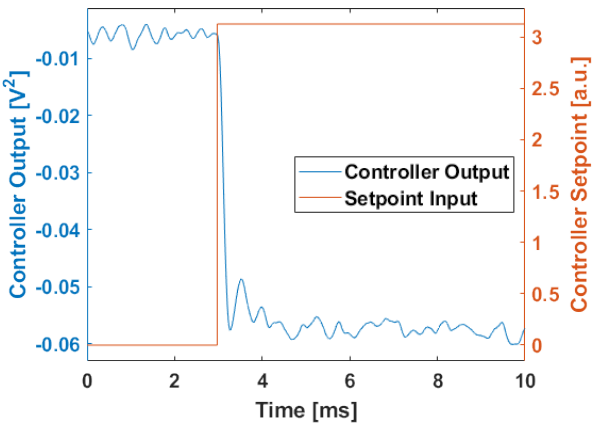

Fig. 2: Controller response to step input in set-point signal. Control loop settles in approximately 1 ms. Dithering amplitude is set to 0.02nm.

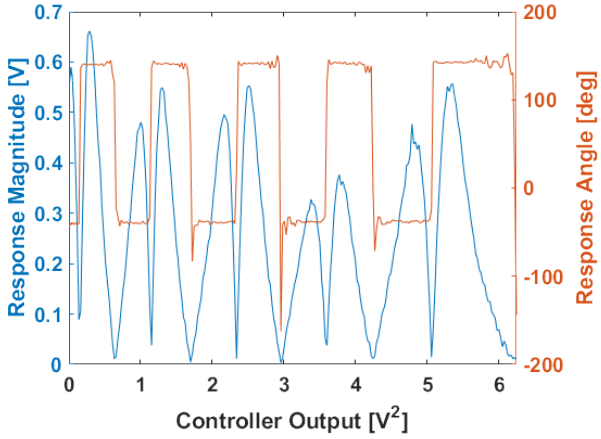

Fig. 3: Calibration Detector output versus control output, dithering amplitude set to 0.02nm. +180-degree phase changes occur at alignment to an optical signal.

thermal control system is implemented on a Terasic TR4 FPGA using custom designed DAC and ADC expansion modules.

In the dithering thermal control system [4], each ring filter is thermally stabilized using a unique control signal, on which a sine wave from a local oscillator (LO) is superimposed. The sine wave has a small amplitude, and each ring is assigned a unique frequency ranging from 20 to 90kHz with 10kHz spacing. The dithering response of each ring to these sine waves is measured by a single photodiode. The measured signal passes through a high pass filter, leaving only the high frequency responses of the dithering. The FPGA employs synchronous envelope detection using each ring's LO to isolate its dithering response. This turns a single feedback signal into eight unique feedback signals. The control loop operates at 500KS/s. This relatively low sample rate allows the FPGA to use the same hardware resources for each channel. The digital controller was implemented using MATLAB's HDL generator, and it contains an integrator, lead-lag compensator, low pass filter, and two notch filters at 10 and 20 kHz.

Because the resonance shift of the ring filters is linear with the power dissipated in the heaters, a purely sinusoidal dithering signal becomes distorted and the resulting dithering amplitude depends on the control signal. To linearize the output of the system and the dithering signal, the square root of their sum is taken. This creates extra frequency components in the voltage signal that the DAC's sample rate must be able to accommodate, but the dissipated power in the ring is a pure sine wave.

2.1. Calibration

The synchronous envelope detection requires phase alignment between the dithering response and the LO that it is mixed with. To calibrate the dithering phase and initialize the control signal to the desired wavelength, we use asynchronous complex envelope detection by mixing the feedback signal with a 90 degree phase shifted version of the LO, implemented by the red blocks in Fig. 1. This then allows us to calculate the magnitude and phase of the feedback signal. Fig. 3 shows the calibration signals versus a scan of a ring's control signal. Identification of the correct signal to tune to can be done using similar methods as demonstrated in [5].

Because higher dither frequencies are attenuated by the thermo-optic lowpass behavior of the micro-ring, the dithering amplitude at high frequencies needs to be larger so that the rings dither the amount in the optical domain. We measured the thermo-optic bandwidth of this PIC to have an approximate behavior of a single pole low pass filter with a cutoff frequency of 76kHz. This model is used to compensate for the attenuation by increasing the dithering amplitude for higher dither frequencies.

3. Measurement Results

To verify control loop stability, we inject a step function on the set-point input of the controller and measure its response. The control loop achieves a settling time of approximately 1 millisecond, as shown for one ring in Fig. 2. Increasing the control loop's bandwidth is possible. However, because the dithering approach results in feedback signals akin to double-sideband amplitude modulation, setting the bandwidth too high results in crosstalk between the control channels. The tradeoff between control bandwidth and number of rings on the bus will depend on each implementation's requirements. To measure the impact of the dithering, we measured the BER of the system with eight parallel 10Gb/s PRBS31 streams. Each data point was taken over a 6-minute period. The results in Fig. 4

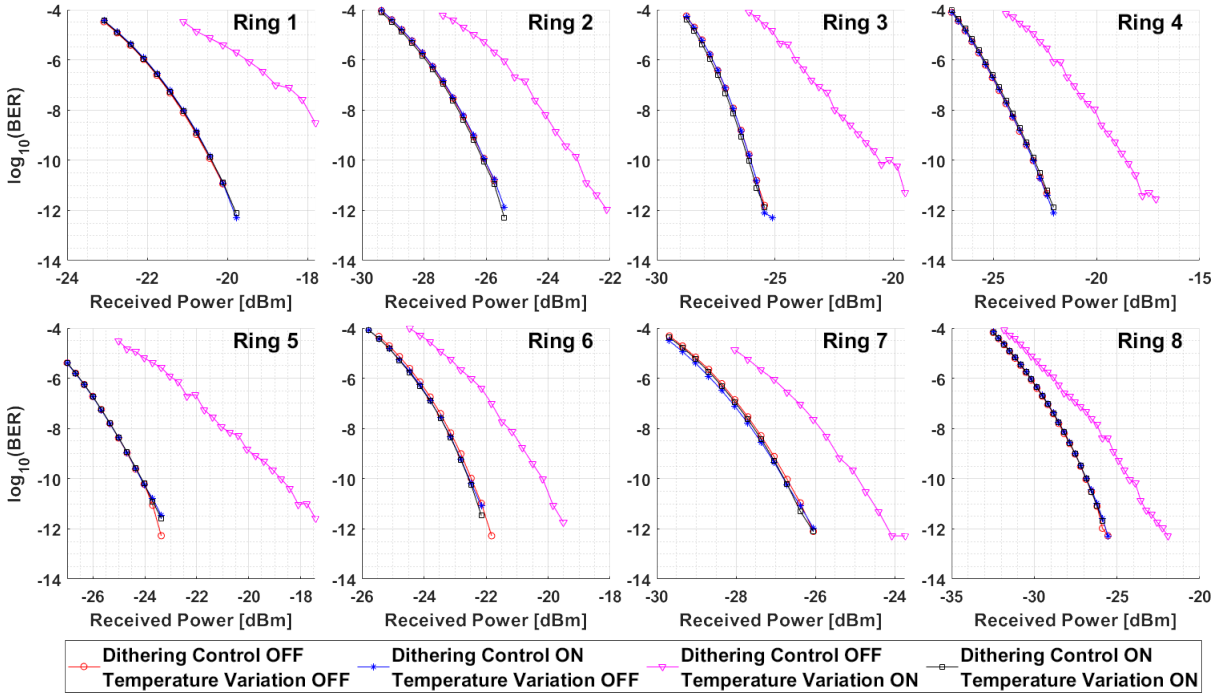

Fig. 4: 10Gb/s PRBS31 BER curves measured on all rings for 6 minutes. Measured with dithering control on and off, with a dithering amplitude of 0.02nm when on. The PCB temperature was kept stable at 27°C by a heater placed next to the PIC, or a thermal variation was forced. When thermal variation was on, the heater was set to 50°C for 90s, then 27°C for 270s.

show that for a dithering amplitude of 0.02nm, the impact on BER is negligible and less than 0.1dB. To force a thermal variation and stress the control loop, we placed a heater on the Printed Circuit Board (PCB) next to the PIC. This variation was enough to severely impact each channel when the control loop was inactive. With the control loop enabled, however, there was negligible difference with the measurements done at a constant temperature.

4. Conclusion

In this work we demonstrated a thermal stabilization architecture based on dithering for cascaded MRR filters. Without using multiple photodiodes and their associated large electrical connections, the dithering architecture creates unique feedback signals for each MRR. This enables stable closed-loop thermal control of compact cascaded ring circuits, while having less than 0.1dB power penalty on BER. By operating mostly in the digital domain on relatively low frequencies and sample rates, the system allows for great flexibility on control design, calibration, and initialization routines.

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References

1. S. Daudlin *et al.*, "3D-Integrated Multichip Module Transceiver for Terabit-Scale DWDM Interconnects," in *OFC 2021,* (2021), p. Th4A.4.
2. D. Y. Lee *et al.*, "Error-free operation of a polarization-insensitive 4λ x 25 Gbps silicon photonic WDM receiver with closed-loop thermal stabilization of Si microrings," Opt. Express **24**, 13204–13209 (2016).
3. P. Dong *et al.*, "Simultaneous wavelength locking of microring modulator array with a single monitoring signal," Opt. Express **25**, 16040–16046 (2017).
4. K. Padmaraju *et al.*, "Wavelength locking and thermally stabilizing microring resonators using dithering signals," J. Light. Technol. **32**, 505–512 (2014).
5. M. Hattink, Z. Zhu, and K. Bergman, "Automated tuning and channel selection for cascaded micro-ring resonators," in *Metro and Data Center Optical Networks and Short-Reach Links III,* , vol. 11308 (SPIE, 2020), pp. 160 – 168.