MicroLED Array-based Optical Links Using Imaging Fiber for Chip-to-chip Communications

Bardia Pezeshki, Farzad Khoeini*, Alex Tselikov, Rob Kalman, Cameron Danesh, and Emad Afifi
*AvicenaTech,, 1130 Independence Ave, Mountain View, CA94043, *ECS Department,University of Michigan, Ann Arbor MI 48109*
bardia@avicena.tech

Abstract: We demonstrate high density (2Tb/mm^2), very low energy per bit (<2pJ/bit), high sensitivity (<-21dBm), and low crosstalk (<-20dB) in various configurations for optical transmission using high speed blue LEDs and integrated photodetector/amplifiers fabricated in 130nm CMOS process.

1. Introduction

High speed GaN microLEDs have recently attracted attention for data communication for LiFi and chip-to-chip applications [1]. Designs optimized for speed can have electro-optical bandwidths that are many GHz and can carry data at 10Gb/s per lane with simple equalization [2]. This is above the clock speed of most silicon ASICs and their internal transfer rates, and suitable for chip-to-chip applications. Leveraging the display industry which has developed the technology to build large arrays of microLEDs and transfer them onto glass or silicon driver chips at high yields, we proposed a new architecture for data communication. The concept, shown in Fig. 1, would use either a separate transceiver chiplet, or an integrated approach, to drive an array of LEDs at high speed and receive signals with integrated photodetectors. Hundreds of lanes can be carried using an imaging fiber [3] at very high density. Such a wide optical bus can connect to other ASICs or memory without the normal latency and power consumption associated with SERDES-based electrical links and release the current data bottleneck in advanced computing systems.

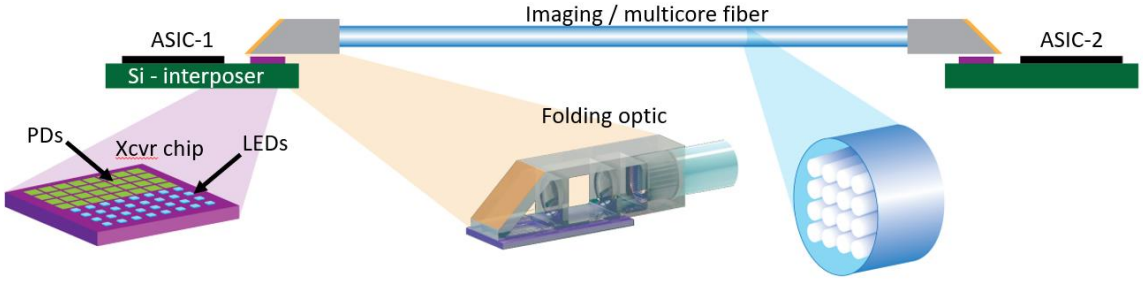

Fig. 1. Concept: The transceiver chip translates electrical data from the ASIC to a wide optical bus with a large array of light emitters and receives signals with an integrated photodetector/TIA array. A large number of beams are carried by a multi-core or imaging fiber through an optional folding optic.

One advantage of using short wavelength light is the high performance that can be obtained with integrated photodetector/TIAs in silicon. The short absorption length of blue light in silicon enables photodetector structures that have very low capacitance per unit area. The low capacitance allows high gain in the TIAs and very low power consumption, while the large area eases alignment tolerances and thus reduces packaging cost.

In this work we demonstrate 256 lanes in a plastic imaging fiber with low crosstalk, and RF data for 8 channels. Fabricating an integrated low-capacitance photodetector with the associated amplifier in an older 130nm process, we show an extremely low power optical link.

2. Experiments.

To show the high density achievable in this technology and to investigate crosstalk impairments, we fabricated both a 16x16 array that was matrix addressed, and also an individually addressed 8 element array of emitters. In both cases, the GaN LEDs were fabricated on patterned sapphire substrates and patterned into 4µm wide mesas. A plastic imaging fiber with a diameter of 1mm and individual core spacing of 10µm (about 7,500 cores) was butt-

coupled onto the array and crosstalk measured in a variety of ways. The left side of Fig. 2 shows the 16x16 array through the 1mm diameter imaging fiber. A 32µm detector was then aligned to a 2x2 subarray through the plastic imaging fiber as it had roughly the same diameter. We then activated the adjacent 4x4 array and measured the relative power received. The experiment was also conducted with a single emitter. The data, shown in the right-hand side of Fig. 2 shows that the crosstalk of the 4 spot subarray is better than 20dB from the adjacent subarray. Moving two arrays, the number drops to better than 25dB. With single elements, the adjacent crosstalk is measured to be better than 25dB. These devices were still on the sapphire substrate and not transferred to silicon, and therefore there was considerable emission and scattering backwards into the transparent sapphire substrate. This is evidenced in the image shown in Fig. 2 with the blue hazy circle around the array. With lifted-off devices that have back reflectors, there would be no such scattered light and we would expect even lower crosstalk.

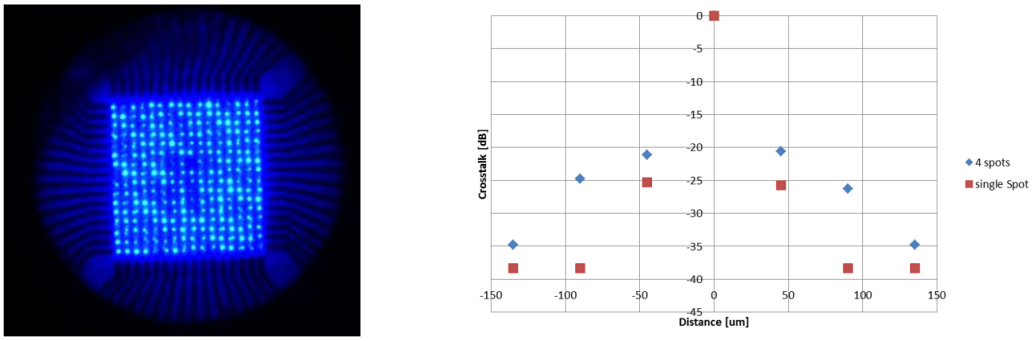

Fig. 2. 16x16 array of 4um diameter emitters, with 30µm spacing as seen through a 1mm plastic imaging fiber. DC cross-talk was measured from 4 illuminated spots to an adjacent detector and from a single illuminated emitter to other detector.

The crosstalk was also measured electrically using the 8-element array with also about 30µm spacing, shown schematically in Fig. 3. In this case an array of silicon photodetectors using 8 commercial TIAs was coupled to the other side of the plastic imaging fiber, and 8 separate bit streams were generated with a Xilinx FPGA at 2Gb/s per lane, the BER was measured with one channel on, and also with all channels on. Once again, because the devices were not lifted-off, there was considerable backscatter from the devices causing about 0.4dB crosstalk penalty.

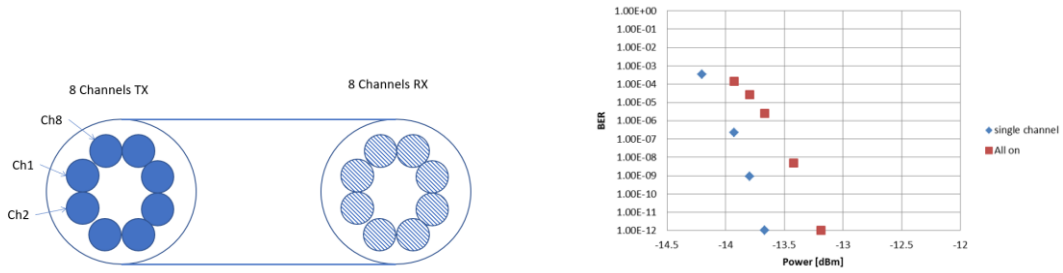

Fig. 3. 8 channel emitter array and photodetector array used to measure crosstalk. 8 commercial TIAs received the signals simultaneously the impairment measured with all channels on.

To demonstrate the very low power consumption achievable with this approach, we fabricated an integrated lateral photodetector coupled to a linear TIA and limiting amplifier using XFAB 130nm CMOS process [4]. The detector used a lateral p-i-n structure that has about 10fF capacitance for a 15µm diameter active area. To measure the bit error rate, an additional low impedance 50 Ohm buffer was also fabricated on chip. The light source for the measurement was a single 15µm diameter LED that was lifted-off onto a silicon substrate with a back mirror and biased at about 0.7mA of current (about 4V), modulated with a PRBS signal. The light from this LED was passed through a variable attenuator and coupled to the detector, generating about 1µA of photocurrent with no attentuation. The total power consumption of the light source at 2Gbps is about 1.5pJ/bit, while the entire receive chain, not

including the 50Ohm buffer was at 0.5pJ/bit. Thus, the total link power consumption was under 2pJ/bit. The eye diagram in Fig. 4 shows the receive electrical eye from the 50 Ohm buffer. The right hand side is the waterfall curve, showing 1E-9 BER at a sensitivity of better than -21dBm.

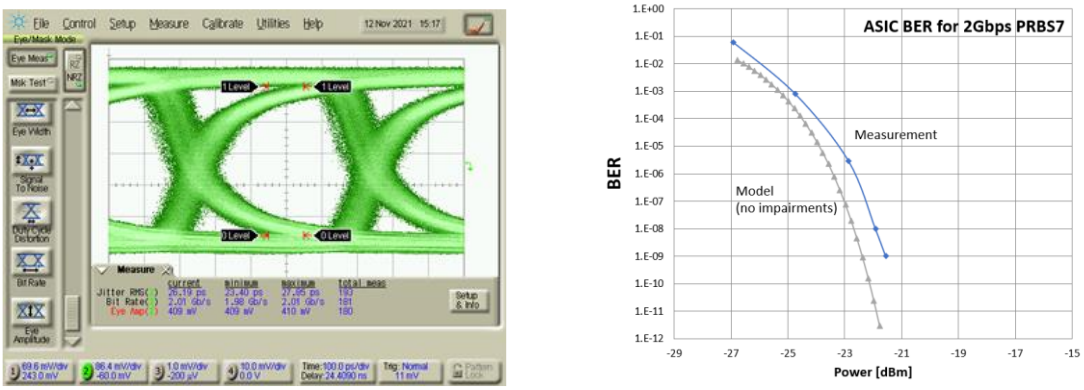

Fig. 3. Received electrical eye and waterfall chart showing link with integrated PD/TIA made in 130nm process. Total power consumption including driver and receiver, (not including the 50 Ohm drive) was <2pJ/bit.

Driving the LED at high current levels, and reducing the speed improved the BER down to below 1E-14. In general, we do not observe any BER floors, which is expected with LED-based links. Unlike laser-based optical links that suffer from the deleterious effects of the coherence, such as modal noise, reflection, and conversion of frequency noise to amplitude noise due to interferometric effects, LED-based links are much more robust. The emission spectrum of the LEDs is about 20nm wide at the center wavelength of 420nm, and LED-based links do not require isolators, polarization control, or sophisticated modulation or error correction. This is critical in interconnects such as inter-processor or processor to memory where BER below 1E-18 and very low latency is desired.

In comparison, other optical transceiver-based links are generally >10pJ/bit, while even the most advanced silicon photonics links aim for 5pJ/bit [5]. Though the reach of single-mode fiber-based links far exceeds what can be achieved with LEDs and plastic fiber, the silicon photonics or single mode technology may be overkill for short distance applications. In this demonstration, the link margin was not optimal, and thus the LED was driven quite hard. By improving the coupling, the LED structure, including an optimized optical coupling element, back reflector, and some light extraction techniques, there is 10dB to 20dB that could be gained. On the receive side, an optimized process on a more advanced node would dramatically reduce the receive power consumption.

Thus by properly optimizing the microLEDs and the receivers in an advanced node, LED based technology should achieve total power consumption approaching or even below 0.1pJ/bit, and costs an order of magnitude lower than other optical or electrical approaches, which is useful for shorter distance data interconnects.

3. Summary

We show that even simply packaged microLED arrays can exhibit very large density for data transfer and low crosstalk. This was measured both in DC and AC formats. The short wavelength is ideal for integrated silicon detectors with TIAs, resulting in very low power consumption, even in a relatively modest 130nm process. Such an approach can provide high density, low power consumption, and time-of-flight-limited latency for advanced computing applications.

4. References

[1] S. Rajbhandari et al., “A review of gallium nitride LEDs for multi-gigabit-per-second visible light data communications,” Semicond. Sci. Technol. **32** 023001 (2017).
[2] B. Pezeshki et al., “Wide and parallel LED-based optical links using multi-core fiber for chip-to-chip communications,” Optical Fiber Conference (OFC 2021)
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[4] F.Khoeini et al., unpublished.
[5] M. Wade et al., “An error-free 1Tbps WDM optical I/O chiplet and multi-wavelength multi-port laser,” Optical Fiber Conference (OFC 2021).