Coherent DSP and System Integration Technologies for 800G

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Abstract: This paper discusses challenges in achieving low-power coherent pluggables for 800G, and innovations required to overcome those challenges. Recent progress in the areas of system integration and low-power DSP design and implementation will be surveyed. © 2022 The Author(s)

1. Introduction

The implementation of 800G coherent pluggables achieving 128 Gbaud nominal symbol rate requires not only advances in system integration of DSP and optics, but also dedicated and efficient DSP algorithms to facilitate high signal integrity in a low-power manner. There are two possible system integration paths toward 128 Gbaud that are currently gaining industry attention: discrete-packaging and co-packaging. The former integrates a BGA packaged DSP die and an Indium phosphide (InP) gold-box packaged optics, e.g. an OIF-compliant HB-CDM [1], on a host PCB board with ultra-low loss transmission lines connecting both packages while the latter directly flip-chip bonds DSP and silicon photonics (SiPho) on a single substrate, providing a higher-level integration. Fig. 1 shows exemplary simulated frequency responses of die-to-die RF connection between DSP and drivers/transimpedance amplifiers (DRV/TIA) for both integration options, including models of different packages (PKGs) and PCB/substrate routing traces, etc. Note that the responses of DSP analog frontend and DRV/TIA were not included, also substrate-DRV interconnect was not considered in this exemplary co-packaging model. Clearly co-packaging exhibits lower insertion loss in this regard; however, further analysis on the archivable transceiver performance based on either integration options would require considerations on practical limits and characteristics of optics and drivers, and also on what DSP can come to play to deal with these imperfections, e.g. high Vπ nature of typical SiPho MZMs may lead to higher drivers' nonlinearity. Therefore, in this paper, we will review several key low-power DSP that would enable 800G coherent pluggables at 128 Gbaud.

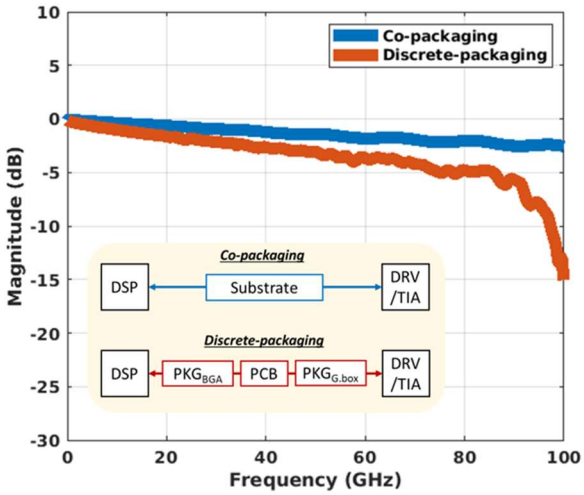
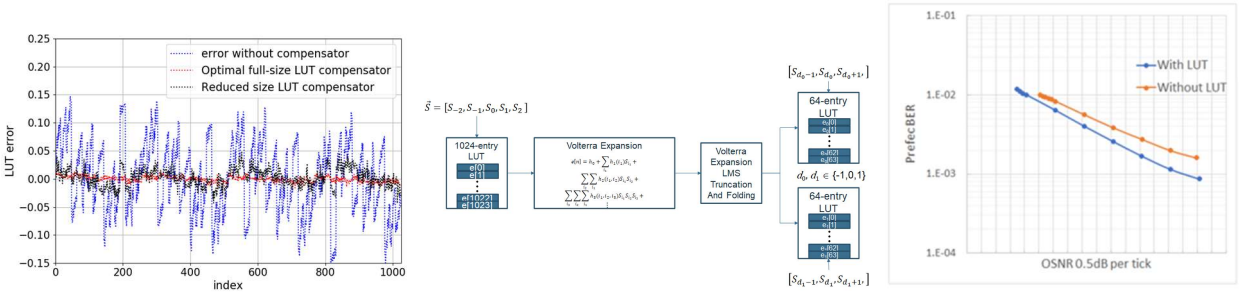


Fig. 1. Exemplary simulated frequency response of die-to-die RF connection between DSP and DRV/TIA for co-packaging and discrete-packaging options, respectively.

2. Enabling Low-Power DSP

2.1. Nonlinearity Compensation



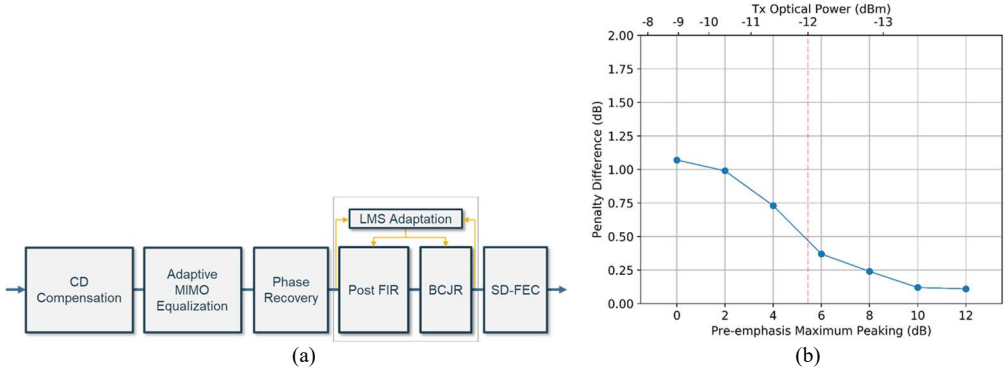
(a) (b) (c)

Fig. 2. A Volterra series based LUT complexity reduction technique for QSFP-DD modules. (a) Nonlinear analysis showing original errors due to nonlinearity and residual errors with 1024-entry LUT (orange) and 2×64-entry LUT (blue), respectively. (b) Schematic diagram of Volterra series based LUT simplification technique. (c) Pre-FEC performance comparison with and w/o simplified LUT.

The low-power and high baud rate requirements also impose the performance limit on optics. It is expected that Vπ of SiPho optics will increase to support higher baud rates, but the driver's power consumption still needs to be low, which severely limits its linearity. The use of look up table (LUT) to reduce devices' nonlinearity is very well known [2]; however, its low-power implementation can be challenging. We have implemented techniques to reduce LUT complexity. As depicted in Fig. 2(a), nonlinearity analysis shows that impairment that extends five QAM16 symbols would require a 1024-entry LUT. One feasible LUT reduction scheme is shown in Fig. 2(b). First, the correction table is expressed as a Volterra series. Then the coefficients are sorted by their amplitudes. The series is then truncated so that the increase of minimum square error with respect to the original error table becomes negligible beyond the truncation. As a proof of concept, a SiPho evaluation board is used in conjunction with an arbitrary waveform generator and a four-channel high speed scope to evaluate the LUT approach for 400ZR. Measurements and analysis showed that the memory of the nonlinearity is concentrated in three symbol sequences around the center symbol. As a result, the 1024-entry table can be reduced to two 64-symbol tables with a programmable lag between them. The comparison of the residual errors after application of the original and simplified LUT are also shown in Fig. 2(a). In Fig. 2(c) we study the LUT performance with the evaluation platform. The LUT provides 0.5 dB OSNR improvement at 1×10^{-2} pre-FEC BER for the same transmit power. We believe that the gain in post-FEC ROSNR will even be greater because the memory of pattern effect can degrade FEC performance, which is reduced by LUT.

2.2. Residual ISI mitigation

To overcome the bandwidth challenges as baud rate of pluggable module increases, partial response equalization technique is being explored as shown in Fig. 3. The partial response is achieved with a noise whitening filter followed by a Maximum a Posteriori (MAP) detector, which is implemented using BCJR algorithm. The partial response equalization technique provides a method to trade-off between noise enhancement and transmitter power that are not available to conventional equalization techniques [3]. Simulation of 800G QAM16 performance for a



(a) (b)

Fig. 3 (a) Block diagram of coherent receiver DSP with partial response equalizer block consisting of a post FIR noise-whitening filter and a MAP detector, and (b) simulated sensitivity difference between pre-emphasis filter and partial response filter with realistic transmitter and receiver model for 800G QAM16 at pre-FEC BER threshold of 2.2×10^{-2}. Note that partial response filter can have as much as 0.45 dB sensitivity improvement at -12 dBm of Tx transmit power.

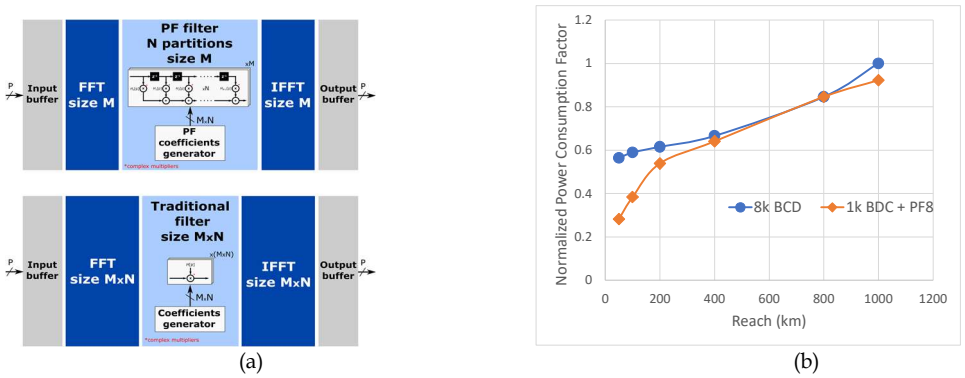


Fig. 4 (a) Architectural difference between traditional (bottom) and Partition Frequency BCD (top) filters and (b) power consumption comparison between the two BCD architectures. Note that the stages in PF BCD filter can be turned off to conserve power to meet the target reach. The traditional BCD filter is not as flexible.

realistic transceiver is shown in Fig. 3(b). The limited Tx bandwidth requires pre-emphasis to reduce ISI at the receiver but at the cost of lower transmitter power. However, the amount of pre-emphasis can be reduced significantly with partial response filtering. At -12 dBm Tx output power, the partial response filter system gives a 0.45 dB in receiver sensitivity improvement. The drawback of BCJR is its complexity. However, various state reduction techniques can be used to reduce its complexity [4]. In Marvell's proprietary implementation, we have managed to reduce the BCJR complexity by a factor 2 with only a 0.1 dB in performance degradation.

2.3. BCD compensation

One of the critical DSP blocks in terms of power consumption is the bulk chromatic dispersion (BCD) compensation filter [5]. For pluggable coherent modules, the DSP needs to support modes with CD ranging from 10's of km to hundreds of km. For BCD implemented in the frequency domain, the FFT size of the filter is determined by the mode that supports the largest CD, which leads to a large power consumption penalty for shorter reach modes. A solution is to use several BCD filters of many sizes, depending on the different application ranges, but that will require large die size and additional power to support interconnection logic of all the filters. A novel solution is to implement BCD using partitioned frequency (PF) filter, as shown in Fig. 4(a). The technique replaces a single stage of filtering with N stages, but the FFT size is also reduced by a factor of N. Each of these stages can easily be turned off according to the desired CD. A power consumption comparison is shown in Fig. 4(b). The normalized power consumption factor is derived from the number of active cells per clock cycle required to compensate a target CD. The power consumption is normalized against the maximum reach of a traditional BCD filter at 1000km. The traditional BCD filter can reduce power by reducing the overlapping factor and clock cycle for a smaller CD target, but the power reduction is gradual and, in this case, such granularity in overlapping factor is not practical. On the other hand, the PF BCD can reduce power at an exponential rate with much finer granularity.

3. Conclusions

In this paper, we presented DSP features to overcome the bandwidth and power challenges to productize pluggable modules at 800Gbps. We presented techniques to overcome transmitter non-linearity when MZM drivers need to compensate for an increase in Vπ. We also presented a BCJR based partial response technique to compensate Tx bandwidth limitation at the receiver without noise enhancement. Finally, we introduced BCD architecture that can tune its power consumption with fine granularity with a large range of CD requirements. All these techniques will help enable 800Gbps pluggable modules in a very bandwidth and power challenged environment.

4. References

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