Glass Interposer for High-Density Photonic Packaging

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Abstract: A circuit on glass with optical fiber interfaces, integrated planar waveguides, and through glass vias is demonstrated for co-packaged optics hosting and interconnecting electrical and photonic integrated circuits by flip-chip bonding.

1. Introduction

High-speed optical interconnects in datacenters and high-performance computers are based on pluggable transceivers. The scaling trend of increasing bit rates and the complexity of the associated electrical circuits increases the power consumption to route the signals between the electrical integrated circuits from the center of the printed circuit board (PCB) to the pluggable transceivers located at the edge. Moving photonic components closer to the electrical switch integrated circuits (ICs) minimizes the power-hungry electrical path length [1] and leads to significant power savings. With serial electrical line rates for 51.2 Tb/s switches expected to increase from 56 Gb/s to 112 Gb/s per lane, heterogenous integration of switch application-specific integrated circuits (ASICs) and photonic integrated circuit (PIC) transceivers onto a common package substrate reduces the electrical interconnect loss by decreasing the required reach from at least 100 mm across the PCB to the front panel to ≤ 50 mm across the substrate package. The decreased reach helps counteract the effects of the higher electrical loss at the doubled Nyquist frequency and is expected to improve the link power budget. The use of photonic interposers for 2D or 3D integration of driving electronic ICs with PICs will further improve power efficiency [2], particularly for high channel count cases. However, there are significant electrical, thermal, and mechanical packaging challenges, particularly resulting from substrate sizes approaching 90 mm × 90 mm and larger for co-packaged optics (CPO). New materials and assembly approaches are needed for: low loss and power efficient high-speed electrical interconnects; thermal management of high-power consuming electrical ICs on the same substrate as temperature sensitive PICs; low substrate warpage, and high electrical reliability of chip-to-package substrate bumps/pillars and substrate-to-board ball grid array (BGA). Glass has a unique combination of properties [3] that makes it well-positioned to overcome these co-packaging challenges. Our approach consists of a single glass substrate where the top redistribution layers (RDLs) connect high-speed electrical lanes between the ASIC and the PIC along with through glass vias (TGV) providing power and ground. The single layer provides simpler fabrication and assembly compared to a 2.5D silicon interposer on an organic substrate or an embedded multi-die interconnect bridge configuration [4] and as such, has the potential for lower overall packaging cost. Glass substrates formed by a fusion draw process inherently have exceptional surface smoothness, as well as the necessary flatness and dimensional stability for small line and space RDLs with tight geometric control, comparable to silicon and far better than organic substrates [5-6]. However, unlike silicon, it can be formed in large formats that contain a high number of package substrates for cost effective, panel-level processing. Glass has a much higher Young's modulus (e.g. ~74 GPa) and hence stiffness than organic materials, and a coefficient of thermal expansion (CTE) that can be adjusted (e.g., 3 to 8 ppm/°C) to match that of silicon or between silicon's CTE and that of a PCB. This provides a package substrate capable of obtaining low assembly warpage and improved solder joint fatigue life. The result of which is high assembly yields and high-power cycling reliability.

2. Substrate with TGVs and Planar Optical Waveguides

Fabrication of ion-exchange (IOX) optical waveguides in 150 mm diameter alkali containing glass wafers is accomplished by performing multiple processing steps including lithography, primary silver ion-exchange, fiducial protection, mask removal, secondary ion-exchange, and laser singulation. Thermal ion-exchange is a batch process where multiple glass sheets can be processed in parallel for scalability and lowest cost. IOX waveguides are planar and are formed close to the surface of the glass with a waveguide loss of less than 0.1 dB/cm and a maximum index difference between the IOX core and surrounding cladding of ~5×10^{-3}. Providing a cavity on a single side of the packaging substrate is key for surface mounting and evanescent coupling of photonic components. IOX waveguides are located underneath the top surface of the glass. The RDL and electrical bumps are inside the cavity to minimize the distance between PIC evanescent couplers and IOX waveguides. The cavity was made by etching 50 µm into the glass to allow enough clearance underneath for the RDL and the electrical bumps. TGVs were formed in glass to connect the top surface inside the cavity with the bottom surface for the glass interposer. Figure 1 shows a schematic

cross-section view of the different process steps starting with IOX waveguide fabrication, cavity and TGV formation, metallization, and PIC assembly. TGVs were etched to an entrance opening of 100 µm and placed with 250 µm spacing inside a 50 µm deep cavity.

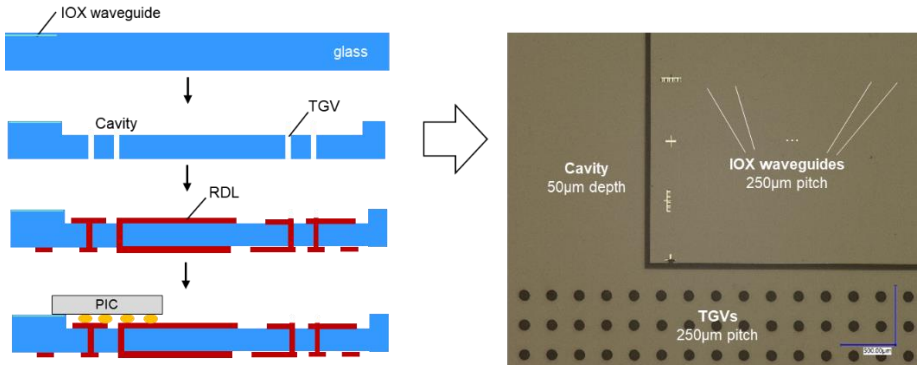

Fig. 1: Process flow of glass interposer fabrication (left) and top-view of IOX waveguides and TGVs inside the cavity (right).

3. Glass Waveguide Connector

The singulation of the glass substrate was achieved using Corning's ultrafast laser nanoPerforation cutting process [7]. The laser modification regions were controlled to avoid damaging the ion-exchange waveguide regions. A mechanical force was applied to separate the substrate along the defined nanoPerforated line. As schematically shown in Figure 2(a), two MPO-16 guide pins were placed inside laser ablated trenches separated by 5.3 mm. The trench width depends on waveguide design and needs to be smaller than the pin diameter to enable the edge alignment. A two-row MPO-16 ferrule compensates for the 250 µm offset between the center of the pins and the waveguide array. Lateral misalignments in the horizontal and vertical directions are driven by the placement accuracy of the trenches in reference to the waveguides and the trench width, respectively. A 0.7 mm glass lid, with the same CTE to reduce the thermo-mechanical stress, was adhesive bonded on top of the guide pins. The adhesive layer thickness was minimized by adding trenches in the lid that are wider than the pin diameter (e.g., 550 µm). Figure 2(b) shows a CPO concept with 16 sets of assembled pins for fiber connectivity along all four etches of the 75 mm substrate. A glass waveguide sample with mated MPO-16 ferrule connector is shown in Figure 2(c). The glass waveguide sample has twelve 15 mm long waveguides which were fiber probed at 1310 nm wavelength yielding an average baseline insertion loss of 0.82±0.07 dB. This insertion loss consists of a Corning® SMF-28® Ultra Optical Fiber to glass waveguide mode-mismatch of ~0.31 dB per waveguide facet and waveguide propagation loss of ~0.1 dB/cm. Then, four different two-row non-angled multi-mode MPO-16 ferrule jumpers populated with Corning® SMF-28® Ultra Optical Fiber were plugged to the pins to compare the fiber probed data obtained with active alignment with that obtained using the passive alignment via guide pins and ferrules. The average insertion loss was measured to be 1.19±0.16 dB for four different MPO-16 ferrule jumpers. Index matching fluid was used at all fiber-to-glass interfaces for characterization. For physical contact, an MPO-16 adapter was designed and assembled on the glass end-facet. The lowest average connector loss was measured to be 0.5 dB [8].

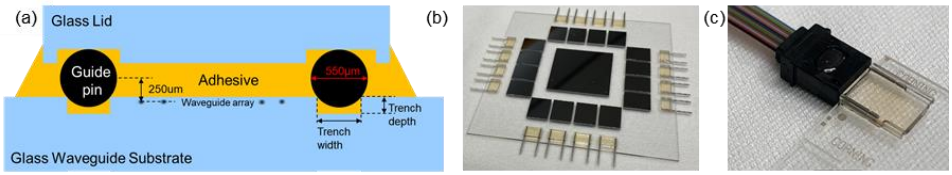

Fig. 2: (a) Schematic cross-section of MPO-16 guide pin assembly on glass, (b) 16 sets of MPO-16 guide pins assembled on a 75 mm x 75 mm glass interposer, (c) MPO-16 ferrule mated with the glass waveguide interface for fiber coupling.

4. Silicon PIC Coupling with Glass Waveguides

Edge and grating couplers are two common methods of interfacing between fiber and on-chip waveguide modes [9]. Recently, evanescent coupling methods (also referred to as adiabatic couplers) that use an intermediary polymer waveguide interposer to connect fiber modes to on-chip waveguide modes have been demonstrated [10]. Such an approach is scalable to high optical port counts and can be automated by pick and place machines. The evanescent coupler assembly stack considered is shown in Figure 3(a). The 500 nm wide, 220 nm thick Si waveguide is tapered

adiabatically in two stages to achieve mode phase matching with the IOX waveguide. A linear taper presents fewer parameters and is less sensitive to variations in the design that accounts for both mode polarizations and a range of wavelengths, simplifying the initial coupler fabrication process considered in this work. Figure 3(b) shows the simulated performance of the evanescent coupler in the 1500-1600 nm wavelength band for a range of adhesive layer thickness values, as deposited on top of the Si waveguide for bonding to the glass. The spectral dependence of the coupling loss for the TE polarized mode is relatively flat in all cases, decreasing for the thin adhesive to less than 0.5 dB across the entire wavelength range. The coupling loss of the TM mode is less than 1.75 dB in the C-band (1530 nm – 1565 nm), with weaker dependence on the adhesive thickness, compared to the TE mode. This leads to a polarization dependent loss (PDL) variation, particularly for thicker adhesive bond lines. The polarization with the lowest coupling loss can change from TE to TM as wavelength is varied, based on adhesive thickness. In general, PDL is expected to be less than 1.5 dB across the C-band. The modeling results correspond to the target design, while the impact of misalignments, additional loss channels, and variations in the coupler material parameters can lead to an increase in the coupling loss. Silicon chips of size 10 mm × 10 mm are fabricated by AMO GmbH in Aachen, Germany, on a silicon-on-insulator wafer with 3 µm buried oxide (BOX) and 220 nm device layer thickness using electron-beam lithography, reactive-ion etching and wafer dicing. For the experiment, IOX glass waveguide samples were aligned to the Si tapers by a set of fiducials and placed by a FINEPLACER® lambda die bonder. After vision-based alignment, the IOX glass is attached to the Si chip and bonded by a UV curing adhesive as shown in top view in Figure 3(c) with an overlap of 3 mm in length. Measurements of the assemblies were made using an external cavity tunable laser connected to the odd channels of a 12-channel fiber array unit (FAU) by an optical switch. After aligning the FAU to the assembly, index matching fluid was used to minimize optical coupling losses. Figure 3(d) shows the measured result for the assembly to be -1.7 dB. The roll-off value was 1.1 dB for both polarizations over the measured wavelength range of 1515-1590 nm. The lowest and highest loss curves are plotted in dark and light colors, respectively. These results demonstrate the potential of glass substrates with high counts of optical waveguides for integration with Si PICs in CPO solutions.

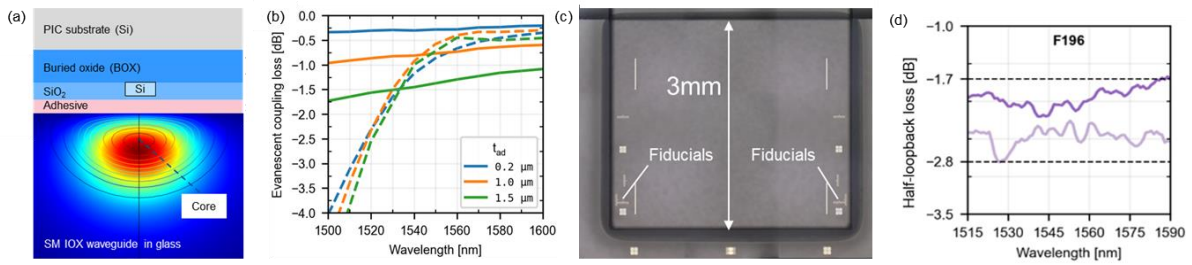

Fig. 3: (a) Cross-section view of stack up, (b) Simulated evanescent coupling loss for 2.5 mm long linear taper for adhesive layer thicknesses (t_{ad}), (c) Top-view of assembled IOX glass waveguides on top of Si PIC with 3 mm overlap, (d) Half-loopback insertion loss including FAU to IOX glass edge coupling and IOX glass to Si PIC evanescent coupling

5. References

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