Performance and Reliability of Advanced CW Lasers for Silicon Photonics Applications

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Abstract: Co-Packaged Optics (CPO) using Silicon Photonics Chiplets in Package (SCIP) is an essential technology for flattening the power consumption curve for Networking and Compute applications in Hyperscale Datacenters. CW lasers are integral to the operation of these systems and are an important part of the power solution. This talk will review the impact of advanced CW lasers on the architecture, performance, efficiency and reliability of CPO systems. © 2022 Broadcom

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Outline

- Energy Efficient Co-Packaged Optics
  - Hyperscale Networking and Compute Growth: Flattening the Power Curve
  - Broadcom SCIP: Advantages over socketed CPO and NPO
- High Power CW Lasers
  - CW Laser Power in CPO Systems
  - CW Laser Characteristics
- Laser Source Technologies
  - Hybrid integration of III-V lasers on SiPh PIC
  - Heterogeneous III-V epi on SOI
  - External Laser Source (ELS)
- Laser and CPO System Reliability
  - Temperature and optical power trade-offs
  - Catastrophic optical damage: laser facets, fiber connectors
  - System Reliability: thermal environment, repairability/sparing
- Standardization Efforts
  - CPO Joint Development Forum
  - OIF CPO Framework and ELSFP Implementation Agreement
  - CW-WDM MSA

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Energy Efficient Co-Packaged Optics

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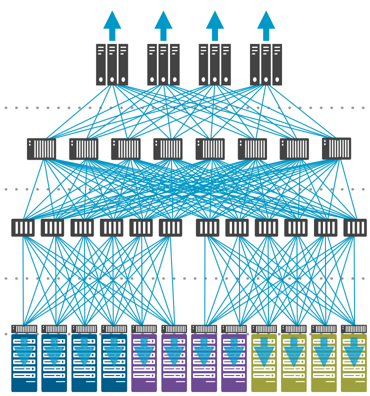
Datacenter Scale-out Requires Massive Fabric Connectivity



>25%

annual growth for intra-datacenter traffic[3]

	Compute and storage resources pooled within datacenter and across regional zones
	Requires long-reach, low-latency interconnects
	Fabric increasing as % spend and **power consumption** of infrastructure

$100B Annual Capex Spend by Cloud with 15% CAGR[1]	19.5 Zettabytes of Cloud Data Movement[2]	Per hyperscale datacenter > 100k Servers > 10k Switches **> 1M Optical Interconnects**

1. 650 Group, Cloud Total Market and Forecast Report
2. Cisco Global Cloud Index, https://blogs.cisco.com/news/acceleration-of-multicloud-era
3. Source: CRN, https://www.crn.com/news/data-center/why-public-cloud-data-center-spending-is-at-an-all-time-high

K. Muth, "Co-packaged Optical I/O with Tomahawk Switch", ECOC, 2021

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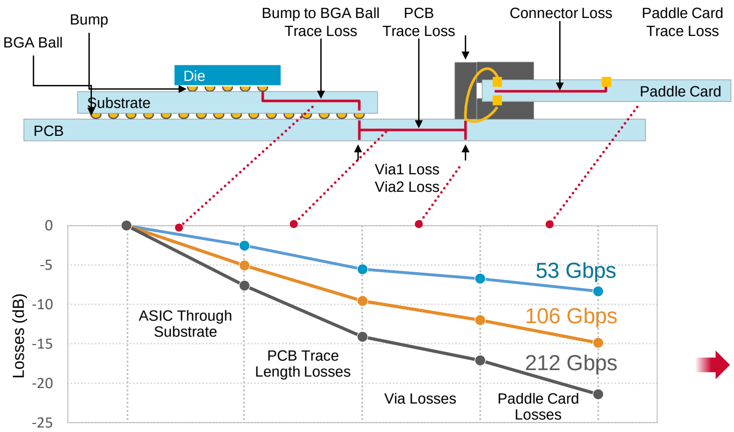
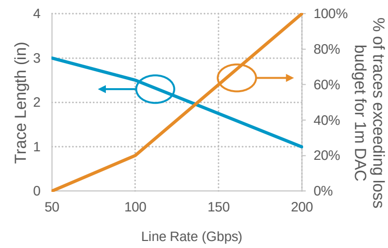
Copper I/O Approaching a Limit



A. Björlin, "Breaking the Bandwidth Barrier: Silicon Photonics Optical I/O", SEMI Americas Virtual Forum, 2021

Each interface in the link between ASIC and Optics adds *analog* loss, requiring additional SerDes Power

The losses grow with each generation of interface speed, but analog efficiency is quickly falling behind Moore's Law.



Simplifying the Connection between ASIC and Optics is Essential to Flatten the Power Curve

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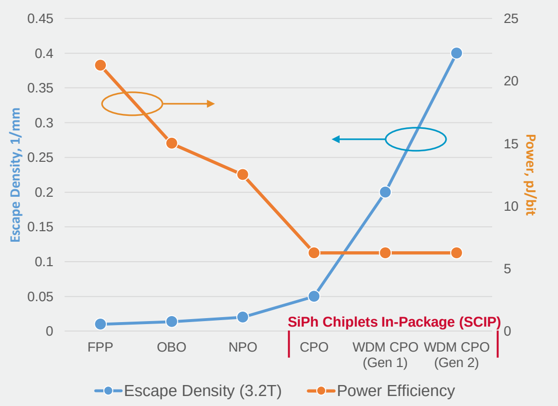
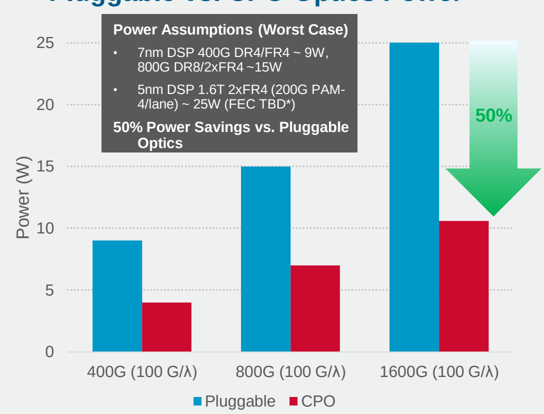
Optimizing Power Efficiency and Bandwidth Density

Escape Density vs. Power Efficiency



Pluggable vs. CPO Optics Power



Exponential Benefit in I/O Escape Density and Power Density with Conversion to CPO

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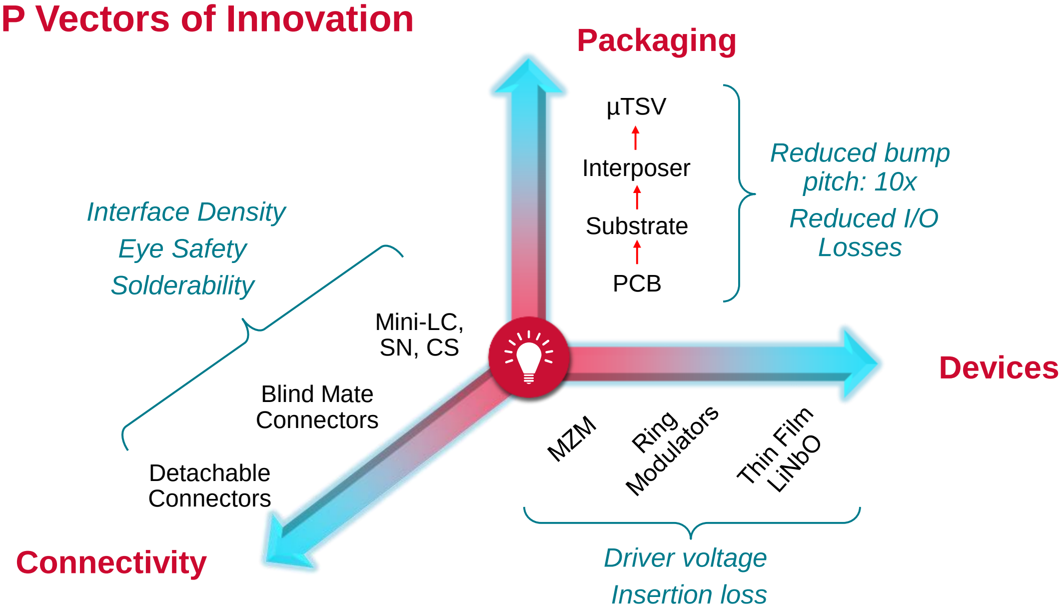
SCIP Vectors of Innovation



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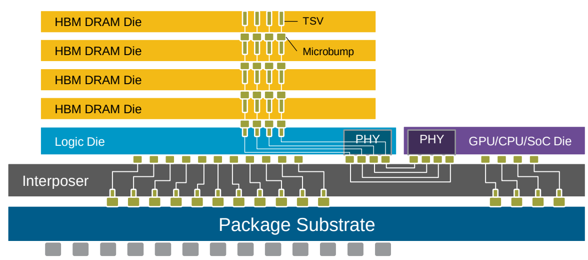
True Co-Packaged Optics

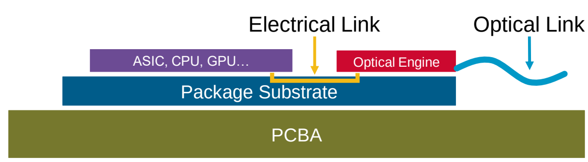
Co-Packaging Already Exists!

- Integration of **multiple dies** on a common package substrate, interposer (2.5D) or die-on-die (3D)
- High volume use cases like High Bandwidth Memory exist today



Co-Packaged Optics

- Integration of **optical engines** on a common package substrate
- Objectives: Alleviate the interconnect density bottleneck and wasted power



A. Björlin, "Breaking the Bandwidth Barrier: Silicon Photonics Optical I/O", SEMI Americas Virtual Forum, 2021

* Source: Image, AMD, https://www.amd.com/en/technologies/hbm
* Source: Yole Developpement, http://www.yole.fr/3D_25D_Stacking_Technologies_IntelEMIB.aspx#.YJyx7pNKh25

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Optics Integration Comparison

NPO, OBO

Optical Engine Characteristics:
- Socketed
- Re-timed
- Grey or WDM

Design Implications:
- Fixed or detachable optical connectors
- Integrated or remote laser sources
- Bandwidth density limited by socket pitch and socket RF characteristics
- Power efficiency limited by equalization and re-timing requirements

Flexibility: Re-configurable, Multi-vendor

SCIP

Optical Engine Characteristics:
- Soldered
- Direct-drive or Re-timed
- Grey or WDM

Design Implications:
- Detachable optical connectors
- Integrated or remote laser sources
- Bandwidth density limited by fiber pitch and λ/fiber
- Power efficiency limited by host ASIC signal characteristics

Efficiency: Power and Bandwidth

SCIP Enables Migration from Serial to Wide-and-Parallel Interfaces: Networking and Compute

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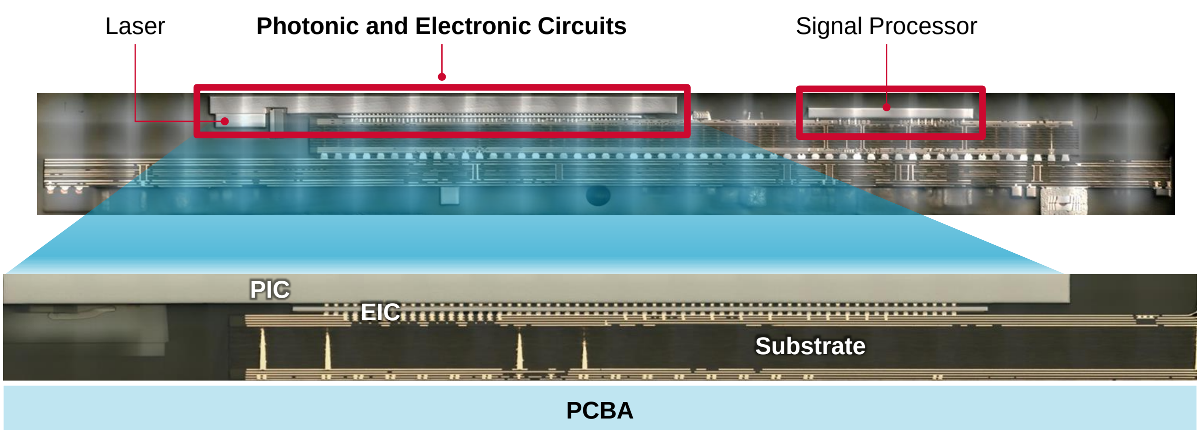
The Anatomy of a Fully Integrated Silicon Photonics Engine



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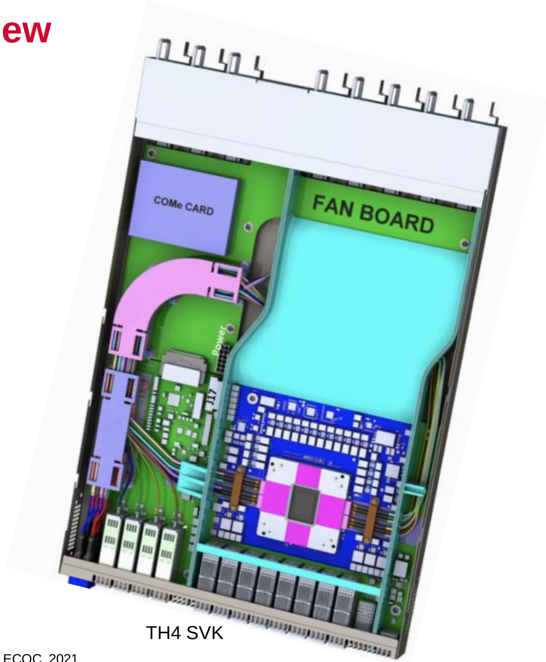
25.6T Broadcom Optical Switch Overview

"Humboldt" (25.6T CPO)

- 25.6T CPO "Half Optics"
- 100GE PAM4 lanes
- 4 x 3.2T Optical Engines
- 4 uncooled ELS w/ Blind mate connector
- 16 x 800G electrical channels for DAC

TH4 SVK early prototype box



TH4 SVK

K. Muth, "Co-packaged Optical I/O with Tomahawk Switch", ECOC, 2021

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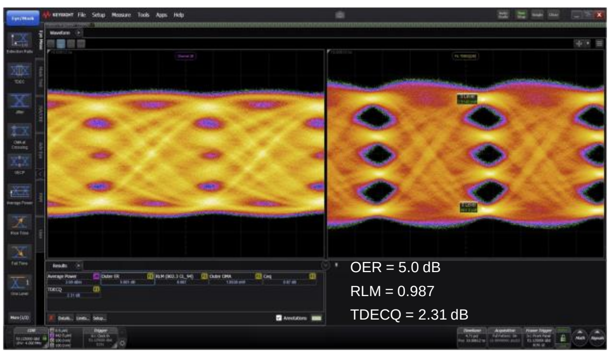
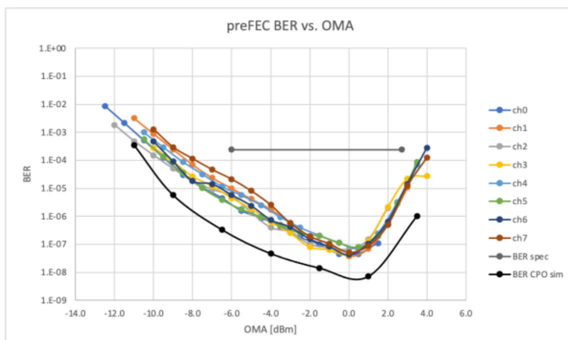
Humboldt Optical Engine – 100G PAM4 Performance

TX PAM4 Eye



RX Pre-FEC BER



OMA normalized to RSSI

Expect ~1dB SNR improvement in final design and elimination of the overload BER degradation

K. Muth, "Paradigm Change in High-Speed Interface Technology", Photonics West, 2021

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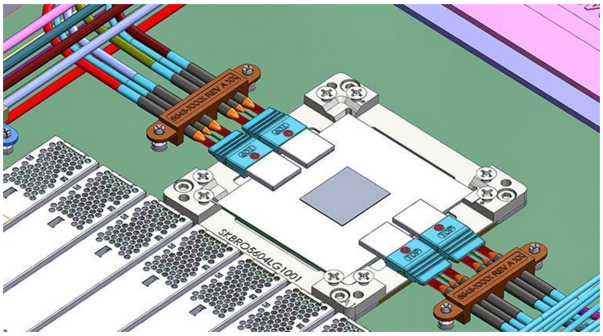
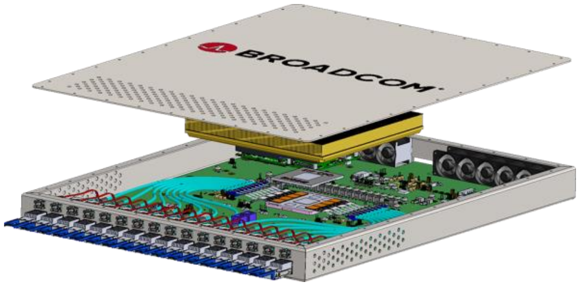
Delivering Disruptive System Value





40% Power Consumption Savings

50% Improvement in Rack Density and Integration Time

40% Lower Optics Cost/Bit

K. Muth, “Paradigm Change in High-Speed Interface Technology”, Photonics West, 2022

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Laser Source Technologies

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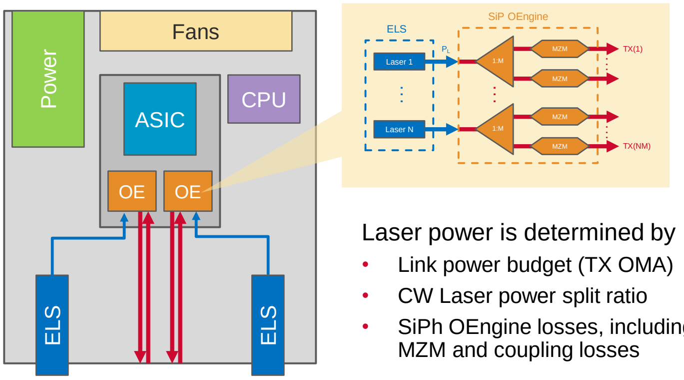
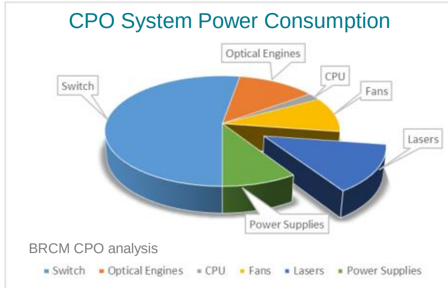
Laser Power in CPO Systems

CPO System Architecture



Laser power is determined by
- Link power budget (TX OMA)
- CW Laser power split ratio
- SiPh OEngine losses, including MZM and coupling losses



- Lasers constitute ~10-20% of system power consumption
- Reducing optics power further reduces PS and fan power!

Source: J. Johnson, "Advanced Laser Technologies in Post-100Gbaud Era“, OFC 2021, Panel Th5C

CW laser source power is a significant fraction of total system power consumption

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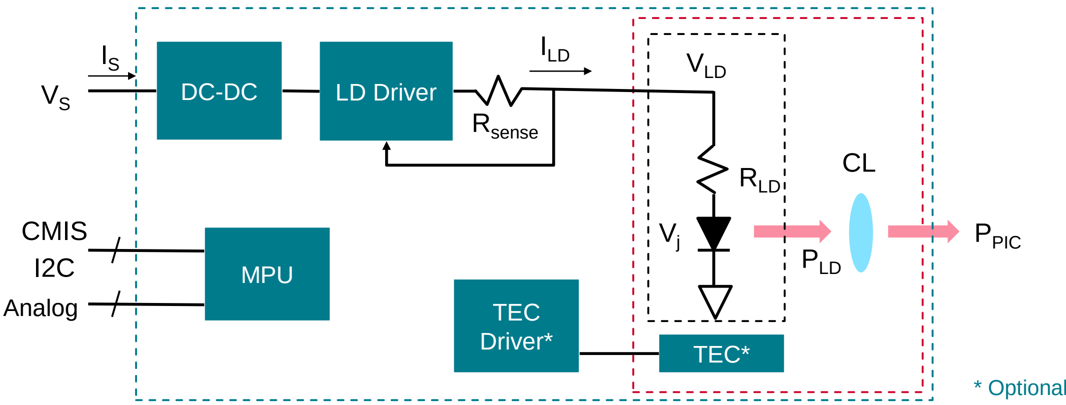
Measures of Laser Source Efficiency



* Optional

Laser diode slope efficiency, $\eta_d = dP_{LD}/dI_{LD}$

Laser diode power conversion efficiency, $PCE_{LD} = P_{LD}/(V_{LD}\, I_{LD})$

Optical engine power conversion efficiency, $PCE_{OE} = (P_{LD}\, CL)/(V_{LD}\, I_{LD} + P_{TEC})$

Module power conversion efficiency, $PCE_{Mod} = P_{PIC}/(V_S\, I_S)$

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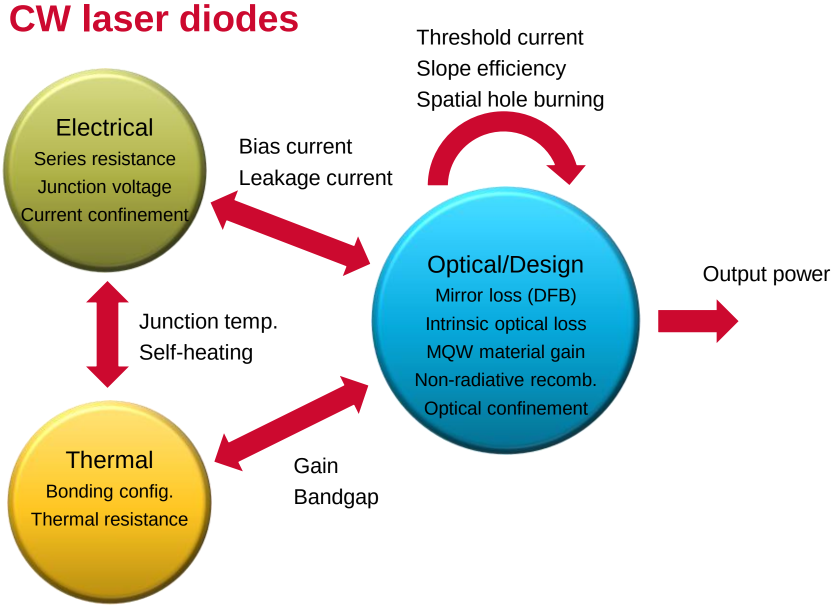
Loss mechanisms in CW laser diodes

Efficient electrical to optical power conversion is a multidimensional, nonlinear problem

- Output mirror loss or DFB grating transmission, longitudinal mode profile
- Intrinsic loss – scattering loss, doping profile, free carrier absorption
- Intrinsic quantum efficiency – MQW quality, non-radiative recombination
- Series resistance – blocking structure, doping, self-heating
- Current leakage – heterobarrier (SCH), blocking junction
- Gain saturation – longitudinal mode profile, optical confinement
- Thermal – thermal resistance, reduced gain, bandgap shrinkage



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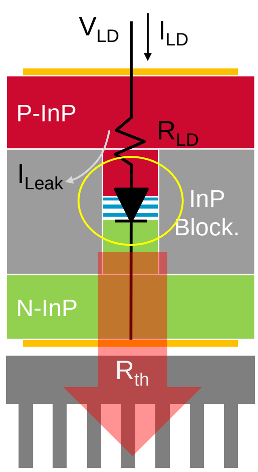
Laser Efficiency Interaction Examples

Higher P-clad doping reduces series resistance, R_{LD}

- ➢ Reduces applied voltage and power consumption
- ➢ Reduces self-heating
- ➢ Reduces leakage into blocking at high bias

Higher p-clad doping also increases inter-valence band absorption

- ➢ Increases intrinsic optical loss
- ➢ Increases threshold current
- ➢ Reduces external slope efficiency
- ➢ Increases operating current
- ➢ Increases self-heating and leakage



Increasing the optical mode confinement

- ➢ Increases modal gain, decreasing threshold
- ➢ Reduces modal overlap with p-InP cladding, reducing intrinsic optical loss
- ➢ Increases gain saturation, spatial hole burning effects
- ➢ Increases far field width, increasing coupling losses

For these reasons, high power CW lasers typically have low optical confinement and longer cavities

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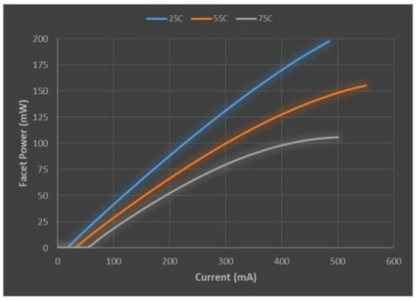
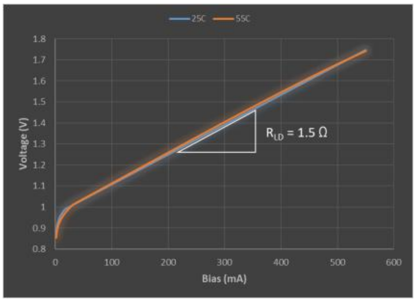
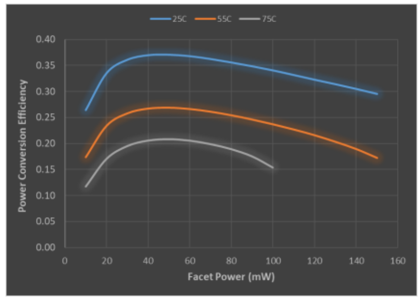
Broadcom 247C CW Laser Power



75mW at 75 °C or 150mW at 55 °C



Low series resistance from CMBH



Highest laser diode efficiency

- CMBH 1310nm DFB laser with MQW active layers, 1 mm length
- Qualified for non-hermetic operation
- Laser is bonded junction-up on a silicon carrier for CW measurement
- Measurement thermal impedance ~ 25 K/W from test fixture to laser junction

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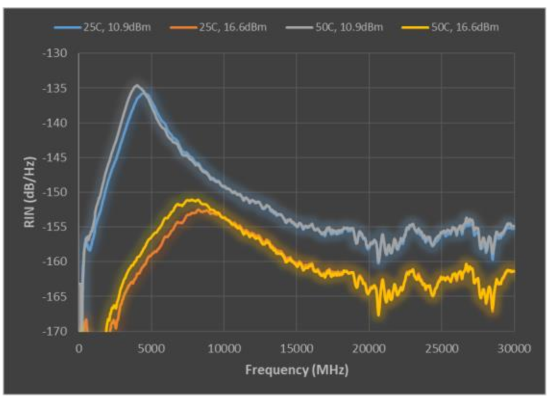
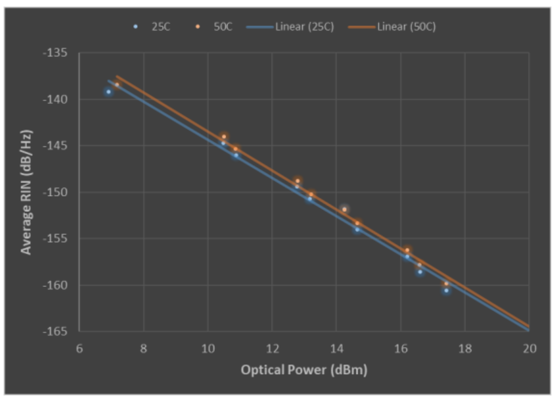
Broadcom 247C CW Laser RIN





- At operation above 16 dBm, average RIN_C is below -155 dB/√Hz
- This is well below the RIN required for 100G PAM4 applications

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Laser Source Strategies for CPO

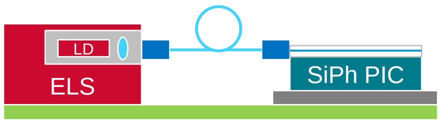
Heterogeneous Integration of III-V on SOI

+ Wafer-Scale Integration
+ Lowest Optical Loss
- No optical isolators
- Close to ASIC: Higher Tj
- Not serviceable
- High R&D investment

Hybrid Laser Attach on Si PIC

+ Existing CM Infrastructure
+ Moderate Coupling Loss
+ Less Scalable than III-V on Si
+ Efficient Native InP Lasers
- Close to ASIC: Higher Tj
- Not serviceable

External Laser Source (ELS)



+ Existing CM Infrastructure
+ Efficient Native InP Lasers
+ Low Tj, Higher Split Ratio
+ Reliable, Repairable
- Higher Optical Loss
- Limited Scalability

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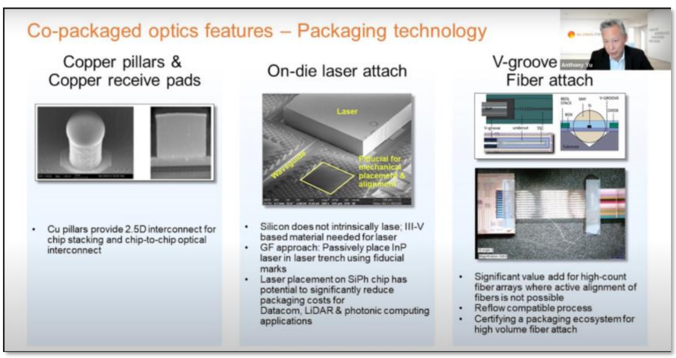
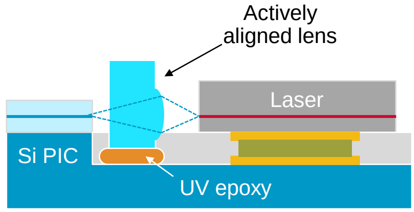
Hybrid Integrated Laser Attachment



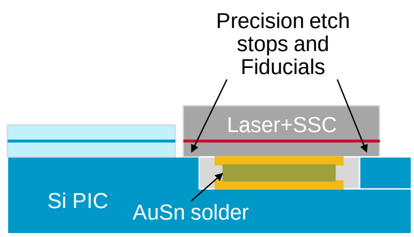
Source: https://semianalysis.com/globalfoundries-is-a-leading-edge-foundry-despite-claims-otherwise/

Hybrid integration uses conventional optical assembly techniques (AuSn, epoxy) and CM infrastructure to align fully-fabricated InP lasers to a SiPh PIC.

Two Integration Approaches:



Active Alignment



Passive Alignment

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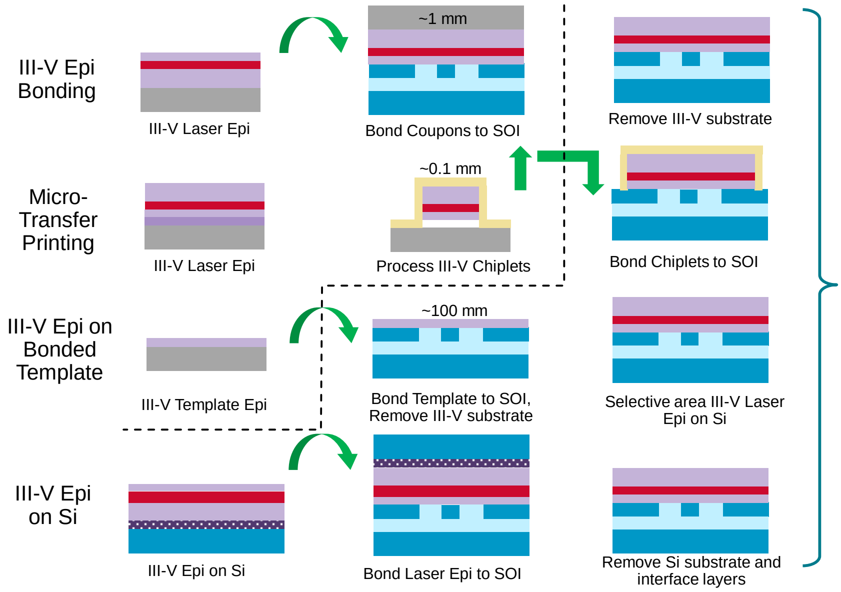
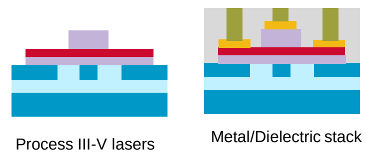
Heterogeneous Integration Process Comparison



Processes to left of the dashed line use small 50-100mm III-V substrates.

Pieces of III-V material are bonded to SOI wafers.



Processes to right of the dashed line are on full 200-300mm SOI wafers, using advanced CMOS processes with excellent process control

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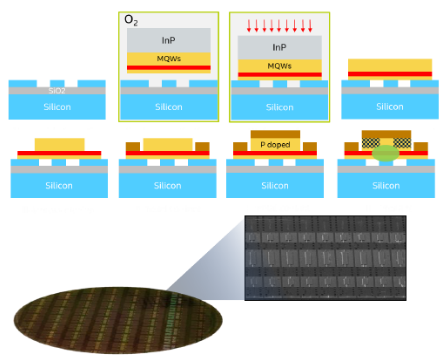
Heterogeneous Integration of InP and Si – Intel

Heterogeneous integration of InP and Si

- Laser fabrication is done after bonding
  - CMOS compatible process flow
  - Take advantage of tight CMOS process control
- Same silicon waveguide used for PIC is used for laser
  - Lasers photolithographically aligned to Silicon Photonic circuit
- IIIV is encapsulated with dielectric
  - No exposed III-V facets
  - Designed for reliability



Compatible with CMOS processing = High volume integration and high yield

Silicon Photonics Product Division FOE 2021 Tokyo intel. 8

Source: Pierre Doussiere, “Recent Progress of heterogeneously integrated InP/Si Photonics”, Fiber Optics Expo, Tokyo, 2021.

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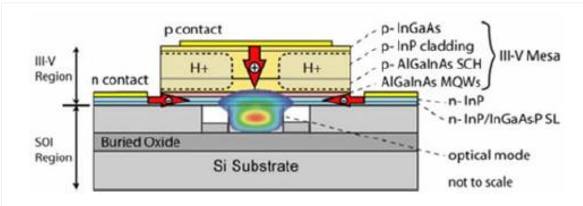
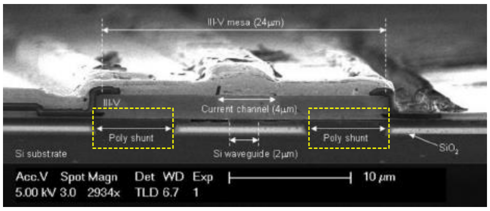
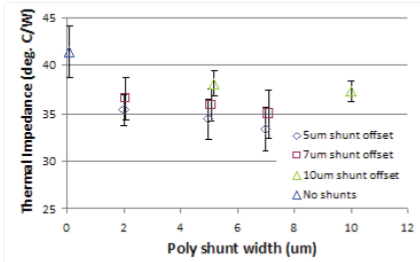
Heterogeneous Integration Challenges





Source: M. N. Sysak, *et al*, "Reduction of hybrid silicon laser thermal impedance using poly Si thermal shunts," *7th IEEE International Conference on Group IV Photonics*, 2010, pp. 296-298,

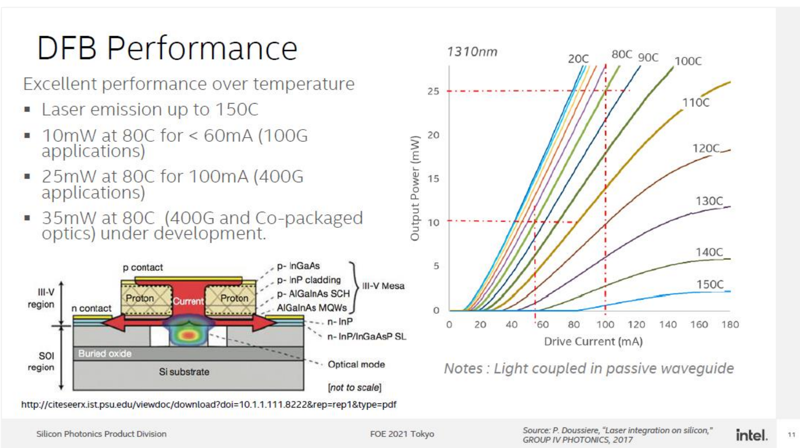


Source: M. N. Sysak *et al*., "Hybrid Silicon Laser Technology: A Thermal Perspective," in *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 17, no. 6, pp. 1490-1498, Nov.-Dec. 2011

Many challenges had to be overcome to bring Heterogeneous Integration to commercial readiness:

- Cross-contamination of Si process equipment by III-V materials
- CMOS-incompatible contact metals (no Au or Pt allowed)
- High series resistance from contacts and lateral injection
- High thermal resistance from BOX → Poly Si thermal shunts

Heterogeneous DFB Performance



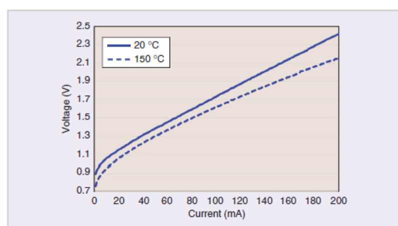


FIGURE 8 The voltage versus current characteristics of a 1,310-nm III/V-Si DFB laser at 20 °C and 150 °C.

Source: R. Jones *et al*., "Heterogeneously Integrated InP/Silicon Photonics: Fabricating Fully Functional Transceivers," in *IEEE Nanotechnology Magazine*, vol. 13, no. 2, pp. 17-26, April 2019.

Source: Pierre Doussiere, "Recent Progress of heterogeneously integrated InP/Si Photonics", Fiber Optics Expo, Tokyo, 2021.

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Tower Semiconductor Announces PH18DA Integration Platform

Tower Semiconductor and Juniper Networks Announce World's First Open Market Silicon Photonics Platform with Monolithically Integrated III-V Lasers

Enables next-generation optical communications for telecoms and datacenters, as well as emerging applications in artificial intelligence and LiDAR for autonomous vehicles

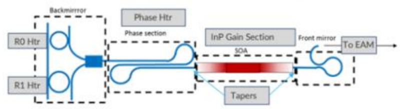
MIGDAL HAEMEK, Israel and MOUNTAIN VIEW, Calif. – December 21, 2021 – Tower Semiconductor (NASDAQ/TASE: TSEM),(NASDAQ/TASE: TSEM), the leading foundry of high value analog semiconductor solutions, and Juniper Networks (NYSE: JNPR), a leader in secure, AI-driven networks, today announced the world's first silicon photonics (SiPho) foundry-ready process with integrated III-V lasers, amplifiers modulators and detectors. This integrated laser process addresses optical connectivity in datacenters and telecom networks, as well as new emerging applications in artificial intelligence (AI), LiDAR and other sensors. According to the market research firm Yole, the silicon photonics transceiver market for datacenters is expected to grow rapidly at a CAGR of 40% to reach over $5B in 2025.

The new platform co-integrates III-V lasers, semiconductor optical amplifiers (SOA), electro-absorption modulators (EAM) and photodetectors with silicon photonics devices, all monolithically on a single chip. This enables smaller, higher-channel count and more power-efficient optical architectures and solutions. Foundry availability will enable a broad array of product developers to create highly integrated photonic integrated circuits (PICs) for diverse markets.

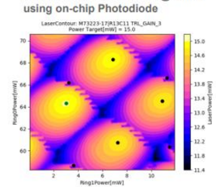
Process design kits (PDK) are expected to be available by year end and the first open multi-project wafer (MPW) run are expected to be offered early next year. First samples of full 400Gb/s and 800Gb/s PICs reference designs with integrated laser are expected to be available in the second quarter of 2022.

Source: https://towersemi.com/2021/12/21/12212021/

Schematic design IIIV-Si Laser Example



Measured Mode Contours @ 15mW using on-chip Photodiode



Tunable laser with passive Si cavity using Vernier-based ring mirrors for mode selection

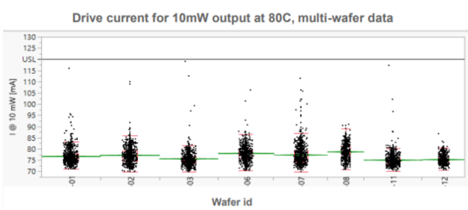
Source: Tower Semiconductor, "PH18DA Overview"

III-V Heterogeneous Laser Integration is Available as a Foundry Platform

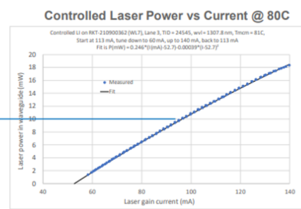
Juniper Networks / Tower Semiconductor Laser Performance

Laser Data

Drive current for 10mW output at 80C, multi-wafer data



Controlled Laser Power vs Current @ 80C



- Typical distribution of laser current required to achieve 10mW of output power
- Data taken at +80C for thousands of lasers on multiple wafers on one lot
- Typical "functional" laser yield on wafers is >97%
- Full laser yield depends on exact specifications being required of the specific laser

- Coupling loss between III-V and silicon is <0.5dB (typical is 0.2-0.3dB)
- >40dB SMSR, RIN < -148dB/Hz, LW ~200KHz
- Passing 2500 hours stressing under following conditions:
    - T_J = 170C
    - J_C = 10kA/cm^2

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Information herein shall not be furnished to third parties or made public

Source: Tower Semiconductor, "PH18DA Overview"

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Heterogeneous Epitaxy on Si

- III-V epitaxy on Si is desired to avoid the cost of III-V substrates, epitaxy and processing on small wafers, and the cost of bonding III-V epi to SiPh wafers
- Growth of III-V directly on Si has many physical challenges due to large differences in material properties that generate defects during epitaxial growth and cool down
  - Lattice constant mismatch
  - Polarity mismatch
  - Thermal expansion mismatch
- Many strategies have been tried to reduce the defect density, and are an active area of research
  - Thermal cyclic annealing
  - Strained superlattice layers
  - Asymmetric graded filter layers
  - Threading dislocation trapping layers
- InAs quantum dot active layers are more tolerant to threading dislocations than quantum wells due to their high local strain field and decreased carrier diffusion length, and are the focus of much III-V on Si heterogeneous epitaxy research
- Quantum dots have other useful properties that are advantageous for optical networking
  - High density of states – Low threshold current density, low temperature dependence
  - Small linewidth enhancement factor – isolator-free operation, narrow linewidth for Coherent and LiDAR
  - Wide gain bandwidth and high 3rd order nonlinearity – mode locked WDM comb sources

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Examples of III-V QD epitaxy on Si

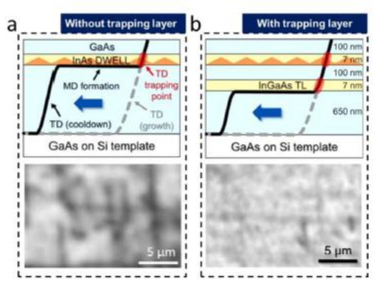

Figure 7. Schematic and the XTEM image of the asymmetric graded filter structure facilitating a higher level of relaxation in the InGaAs filters. The surface TDD is measured with ECCI (TD circled in white) and PVTEM. Schematic representation (upper) and monochromatic CL image (lower) of a QD structure (a) without and (b) with TL designs. The gray dashed lines represent the as-grown defect configuration, and the red ovals suggest pinning points in the active region and in the TL structure. Reproduced with permission from ref 83. Copyright 2020 AIP Publishing.

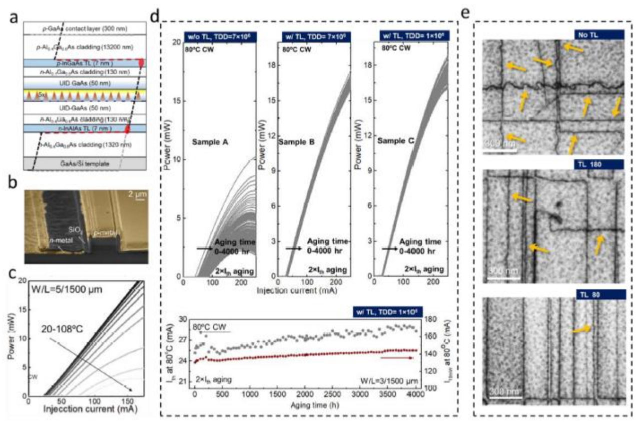

Figure 8. (a) Schematic of the laser stack with the inserted TLs 180 nm away from the active region. The MDs (red dashed lines) would form close to the TLs instead of the active region. (b) SEM images of the device being aged (c) Temperature-dependent $L-I$ curves of the best device incorporating the TL design on 1×10^6 cm^{-2} TDD GaAs-on-Si buffer. (d) $L-I$ curves evolution during the 4000 h aging at 80 °C for different TL designs and TDD GaAs-on-Si buffer, the bottom figure shows aging data (at 80 °C/$2 \times I_{th}$) for the hero device incorporating the TL design on 1×10^6 cm^{-2} TDD GaAs-on-Si buffer. (e) Postaging microscopy analysis for devices with different TL designs. Yellow arrows are pointing to the MDs showing signs of REDC. (a)−(d) Reprinted and adapted with permission from ref 71. Copyright 2021 The Optical Society. (e) Reproduced with permission from ref 70. Copyright 2021 AIP Publishing.

Source: Chen Shang, *et al*, “Perspectives on Advances in Quantum Dot Lasers and Integration with Si Photonic Integrated Circuits”, *ACS Photonics* 2021 *8* (9), 2555-2566, DOI: 10.1021/acsphotonics.1c00707

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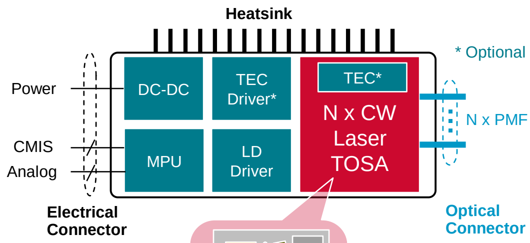
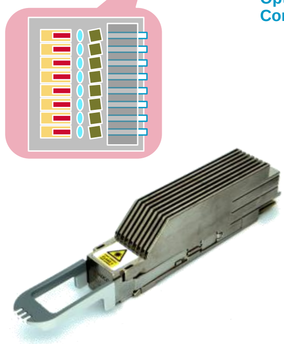
External Laser Source (ELS)

- ELS allows decoupling of the thermal environment of the laser and CPO optical engine and easier management of laser reliability.
  - Lasers on a CPO Chiplet runs hotter than faceplate pluggable client optics due to close proximity to the ASIC.
  - Faceplate pluggable ELS receives the coolest airflow, resulting in highest laser efficiency and reliability
  - Easily replaceable in case of (unlikely) laser failure
- ELS configuration is driven by system capacity, PIC split ratio and laser power at max module case temp
  - 8 x 20 dBm lasers: 16 ELS for 51.2T with 100G lanes (1 RU)
  - 8 x 17 dBm lasers: 32 ELS for 51.2T with 100G lanes (1 or 2 RU)
- High efficiency is required for low power consumption and to minimize carryover heating of ASIC
  - Module and TOSA heatsinking to minimize laser operating temp
  - High Laser Efficiency to operate at lowest possible bias and temp
  - Low Optical Losses – fiber coupling, connector losses
  - Low Electrical Power – Efficient DC-DC and LD driver, avoid TEC
- High optical power (29 dBm total) drives the adoption of interlocks and blind mate connectors for eye safety.





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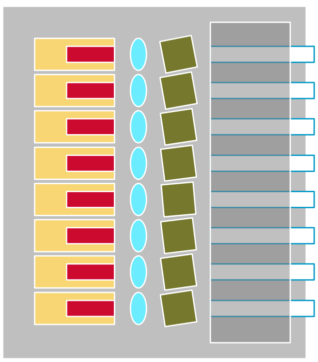
Uncooled vs. Cooled ELS



Approximate size of 8-channel array of CW lasers with lenses, isolators and fiber array on 1.2mm pitch is 12 x 12 mm to fit in QSFP or OSFP width.

- Uncooled lasers will always have the lowest power consumption and highest efficiency at a given temperature.
- Lower power enables operation with $T_{Case} \leq 50$ºC with appropriate ELS heatsink design
- Adding a TEC can reduce the laser temp, but the added TEC power increases case temp. T_{Case} up to 70ºC is likely.
- As a rule of thumb, you need a TEC with > 2x the laser heat load at ΔT=0, but size must fit in the module.
- Several vendors provide online tools for estimating TEC performance, for example:
  - Ferrotec USA model 20013/031/040B
  - Cold plate: 15.1 x 15.1 x 2.9 mm, Q_C(max) = 9.2W at ΔT=0.
  - Assume a TEC of 12 x 19mm with same junction area will have similar performance.
  - Assume TEC hot plate to heatsink thermal resistance = 2 K/W

Source: https://thermal.ferrotec.com/products/peltier-thermoelectric-cooler-modules/20013_031_040b/

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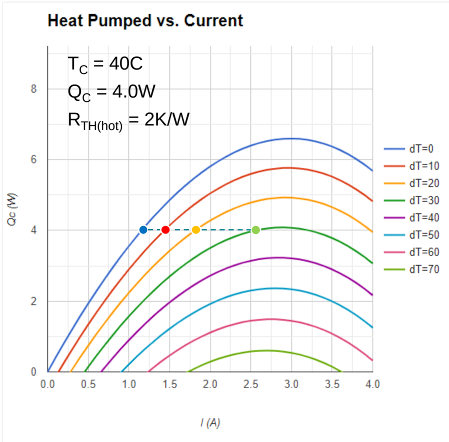
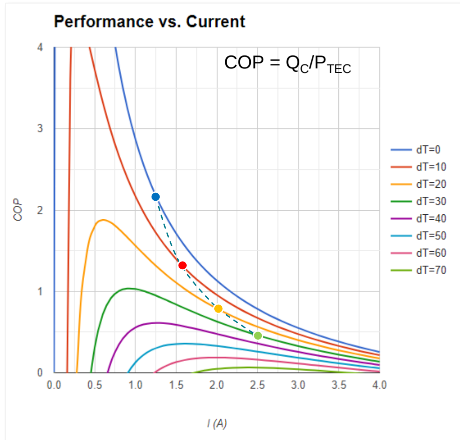
TEC Performance Example





TEC efficiency (COP) degrades rapidly with increasing temperature delta.

Source: https://thermal.ferrotec.com/products/peltier-thermoelectric-cooler-modules/20013_031_040b/

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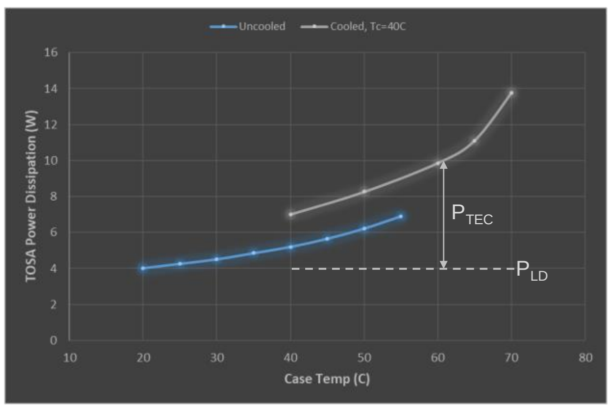
Comparison of ELS Power Dissipation

- ELS TOSA assumptions:
  - 8 CW lasers providing 100 mW per fiber
  - Laser facet power = 149 mW (CE = 1.7dB)
  - Thermal impedances:
    - Uncooled laser junction to case = 25 K/W
    - Cooled laser junction to cold plate = 23 K/W
    - Hot plate to module case = 2 K/W
    - Parasitic heat conduction and convection are ignored (underestimates TEC power).
- Uncooled ELS has TOSA P_{dis} < 6.2 W up to 50ºC max T_{Case}. Beyond ~50ºC, lasers have insufficient operating margin.
- Cooled ELS has TOSA P_{dis} < 14 W up to 70ºC max T_{Case} at ΔT = 30ºC. At ΔT~30ºC, TEC is near thermal runaway limit.



With proper thermal design, uncooled ELS is significantly more efficient.

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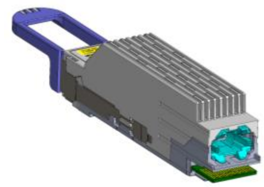
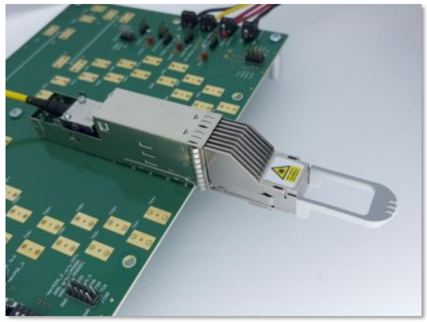
Broadcom Beacon Uncooled ELS

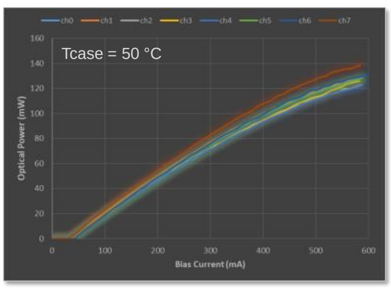
- Uncooled ELS designed for the Humboldt 25.6T and future 51.2T CPO switches
- Supports a 1:4 power split ratio – single ELS per 3.2T optical engine
- Double-height QSFP-DD form factor with large heatsink enables efficient uncooled ELS operation
  - 8 Broadcom 247C lasers produce 20 dBm per fiber at case temperature up to 50°C
  - Total module power dissipation is < 8 W, leading to module PCE > 10%
  - Low carryover heating of switch ASIC
  - Up to 16 modules per 1 RU shelf (512 100G lanes)
- Blind mate PMF MPO connector is required for eye safety: total optical power > 800 mW





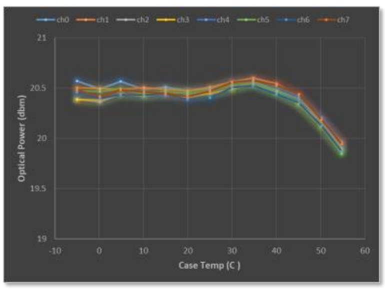
Beacon ELS Results

Fiber-coupled L-I curves



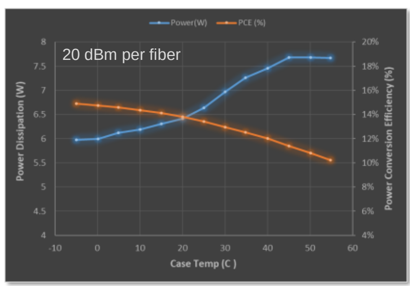
Bias current < 450 mA at 100 mW

Fiber-coupled power



>20 dBm power up to 50°C case

Power dissipation and Efficiency



Module power < 8 W up to 50°C
Module PCE > 10%

To our knowledge, this is the highest optical power and efficiency ELS published to date

Disclaimer: Preliminary paper, subject to publisher revision

Power Budget Comparison

Parameter	Uncooled ELS	Cooled ELS	Hybrid Integration	Heterogeneous Integration
Case/HS Temp (ºC)	50	40	85	85
Thermal Impedance (K/W)	25	25	30	35
Series Resistance (ohm)	1.5	1.5	1.5	6.5
Junction Temp (C)	66.0	52.7	93.4	88.0
Laser current (mA)	465	407	244	68
Laser Pout (dBm)	21.7	21.7	17.2	11.2
Laser Pdis (W)	0.789	0.655	0.333	0.098
PTEC at COP=1 (W)	0	0.506	0	0
Laser PCE (%)	18.9%	12.8%	15.8%	13.5%
Laser-PIC Coupling Loss (dB)	4.5	4.5	3.0	0.0*
Power Split, 1:N	4	4	2	1
WG, Splitter losses (dB)	0.5	0.5	0.5	0.5
MZM Ins. + Mod. Loss (dB)	6.0	6.0	6.0	6.0
Output Coupling Loss (dB)	2.5	2.5	2.5	2.5
OMA (dBm)	2.0	2.0	2.0	2.0
Laser Pdis per TX (W)	0.197	0.290	0.167	0.098
TX Optical PCE (dB)	0.8%	0.6%	1.0%	1.7%

Broadcom data

Intel data

* Included in laser L-I

Same for all cases

Uncooled ELS is the most efficient external laser solution, similar to Hybrid Integration
Heterogeneous Integration is the most efficient, scalable solution in the long run

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Summary of CW Laser Technologies

Parameter	Hybrid Laser Attach	Heterogeneous III-V Epi Bonding	Heterogeneous III-V Epi on Si	External Laser Source	Comments
Coupling Loss	Moderate	Low	Low	High	ELS coupling in/out of fiber
Laser Power	High	Low	Low	High	Native III-V laser efficiency
Operating Temperature	High	High	High	Low	On-PIC laser proximity to ASIC
Power Dissipation per Lane	High	Low	Low	High	Driven by optical losses
Reliability	High	High	Improving	High	Heterogeneous epi defects
Serviceability	No	No	No	Yes	ELS is field replaceable
Scalability	Low	Moderate	High	Low	Si wafer scale is preferred
Multiple Bandgaps (WDM)	Yes	Yes	Limited	Yes	Mix lasers from multiple wafers
Commercial CM Availability	Yes	Yes	Not Yet	Yes	New foundry announcement
R&D Investment	Low	Moderate	High	Low	Heavy investment in III-V on Si

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Laser Reliability in CPO Systems

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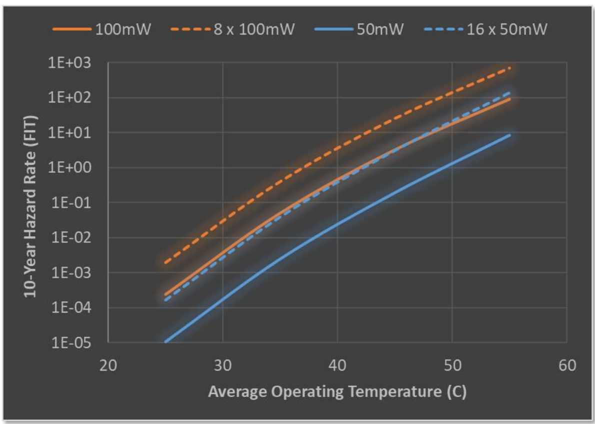
Laser Reliability vs. Output Power and Temperature



16 50mW lasers can have the same reliability as a single 100mW laser due to reduced junction temperature

Source: J. Johnson, "Advanced Laser Technologies in Post-100Gbaud Era", OFC 2021, Panel Th5C

- Laser reliability is exponentially proportional to junction temp, driven by
  - Laser diode efficiency: bias current, output power
  - Optical coupling losses reduce efficiency
  - Series resistance leads to power dissipation
  - Thermal resistance to heatsink increases T_j

$$AF = \exp\left[\frac{E_a}{k_B}\left(\frac{1}{T_{j2}} - \frac{1}{T_{j1}}\right)\right]$$

- Designing for the best laser diode and thermal efficiency yield the highest reliability at any given optical power
- Lower optical power split ratio is one path to improve system reliability
  - Uncooled ELS with efficient BH lasers and low case temp can support power split to 4 lanes
  - Integrated lasers with higher heatsink temp typically support only a single lane
  - Increased laser and interconnect cost

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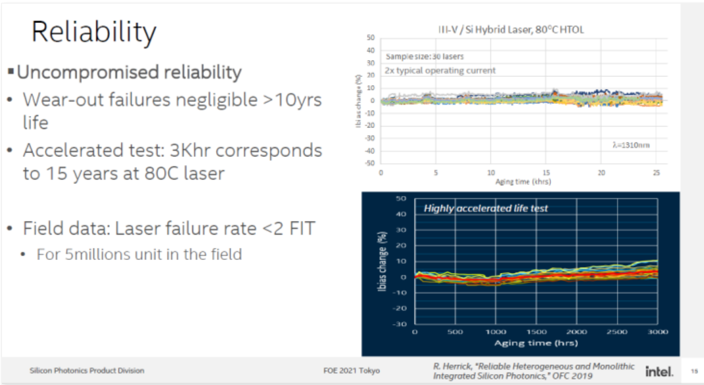
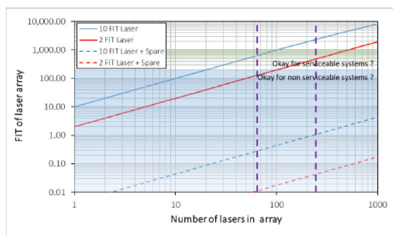
Reliability – Heterogeneous Integration



Source: Pierre Doussiere, "Recent Progress of heterogeneously integrated InP/Si Photonics", Fiber Optics Expo, Tokyo, 2021.



Simulated Laser array FIT; assuming uncorrelated laser failure
FIT = number of failures in 1Billion device hours

- Integrated lasers are not serviceable. A single laser failure brings down the whole switch
- Even with excellent single-laser reliability, system failure rate is high for 25.6T
- Adding a spare laser and protection switch to each channel results in high system reliability, at the cost of additional InP epi material and switch loss.

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CW Laser Source Standardization

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CPO Collaboration Joint Development Forum

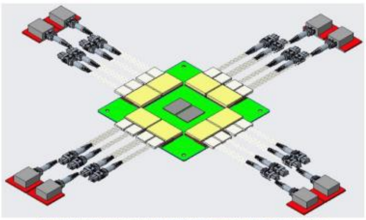

Figure 1: Example embodiment of a 51Tb/s CPO assembly with OBO ELS modules

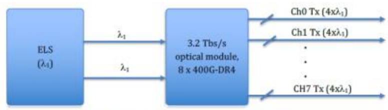

Figure 4: Example of 3.2 Tb/s, 400GBASE-DR4 optical module

Parameter	Symbol	Min	Typical	Max	Unit	Note
Power supply voltage	Vcc1	3.14	3.3	3.47	V	
Operating case temperature	Tcase	20		70	°C	
Power consumption	P			15	W	With QSFP-DD form factor
				20	W	With OSFP or other pluggable form factor
				20	W	With 8x OBO form factor
				40	W	With 16x OBO form factor
Power consumption in Low Power Mode	P_lpm			1.5	W	
Steady state current	Icc			5	A	For max 15W power consumption
				6.5	A	For max 20W power consumption
				13	A	For max 40W power consumption
In-rush, instantaneous peak current	I_peak			Icc max +30%	A	Peak inrush current for the supply rail
Relative humidity	RH	5		85	%	Non-condensing

Table 2: Operating conditions

Description	Value	Unit	Note
Lane wavelength (range)			Ref: IEEE 802.3bs
Side-mode suppression ratio (SMSR) (min)			Ref: IEEE 802.3bs
Average launch power, each lane (max)	27	dBm	See section 4.2.4
Average launch power, each lane (min)	23	dBm	Expected min power accepted in order to minimize input fiber quantity
Average launch power of OFF transmitter, each lane (max)	-15	dBm	
RINc (max)	-141.5	dB/Hz	Note 1

Note:
1. RINc can be calculated from measured RIN_OMA. RIN_OMA can be measured using method in IEEE 802.3ae with 17.1dB reflection coefficient.

Table 4: ELS characteristics for DR4 applications

- Collaboration led by Facebook and Microsoft
- Published guidelines for CPO module and ELS in 2020-2021
- ELS Guidance document describes electrical, optical and thermal requirements for an ELS, including
  - Operating and environmental conditions
  - Optoelectronic requirements and power classes
  - Management interface
- Limited mechanical guidance – reuse of existing MSA form factors

Source: http://www.copackagedoptics.com/wp-content/uploads/2020/01/ELS-Guidance-Doc-v1.0-FINAL.pdf

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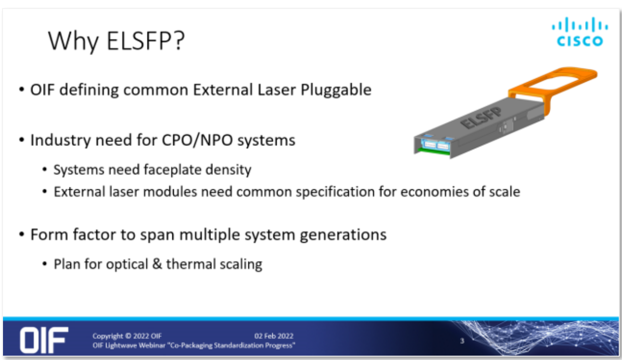
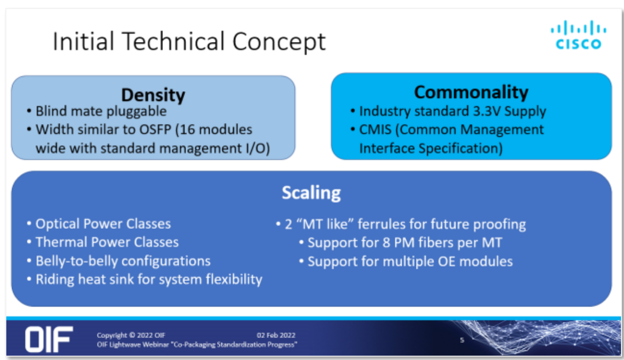
OIF Co-Packaging ELSFP Implementation Agreement





Source: J. Bovington, OIF Lightwave Webinar, "Co-Packaging Standardization Progress", Feb. 2022

As part of the OIF Co-Packaged Optics effort, the ELSFP Project is tasked to generate a more complete Implementation Agreement for a faceplate pluggable module optimized for CW lasers

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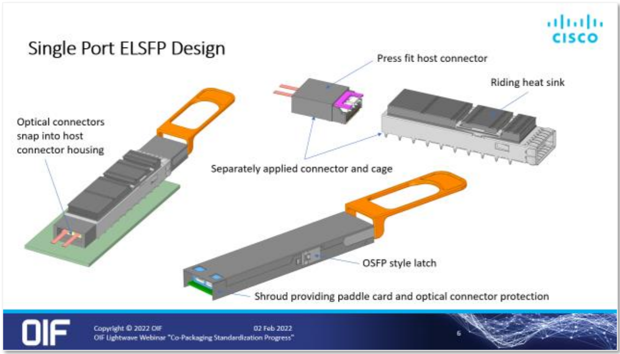
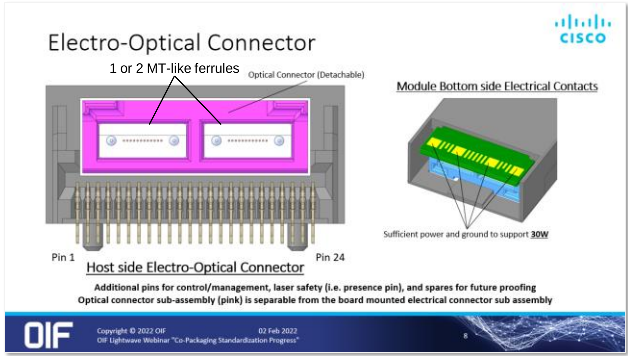
ELSFP Mechanical/Optical





Source: J. Bovington, OIF Lightwave Webinar, "Co-Packaging Standardization Progress", Feb. 2022

- Key features of the emerging ELSFP agreement:
  - Mechanical footprint similar to OSFP, including cage with riding heatsink
  - Blind mate optical connector with 1 or 2 MT-like ferrules, up to 8 fibers per ferrule
- Detailed specification development is still ongoing

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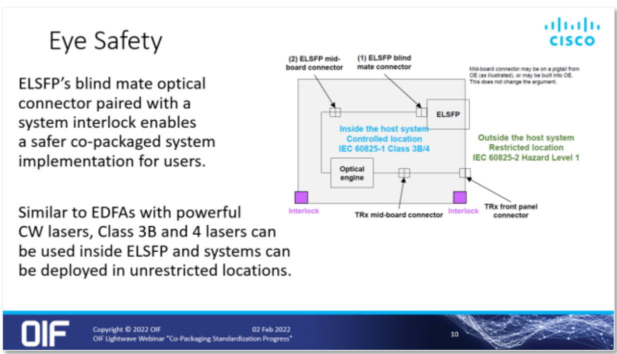
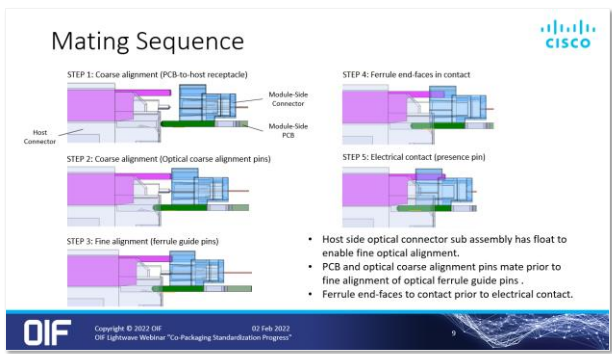
ELSFP Blind Mate Optical Connector





Source: J. Bovington, OIF Lightwave Webinar, "Co-Packaging Standardization Progress", Feb. 2022

- Eye safety is critical for ELS, which can emit more than 1W of optical power
- The blind mate optical connector restricts user access to the powered optical output
- Optical mate before electrical contact adds further eye safety and prevents hot optical mate/demate which can damage the ferrule

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CW-WDM MSA

- "The CW-WDM MSA (Continuous-Wave Wavelength Division Multiplexing Multi-Source Agreement) was formed to standardize WDM CW sources in O-band for emerging advanced integrated optics applications that are expected to move to 8, 16, and 32 wavelengths."
- "Such higher wavelength counts are needed for emerging applications such as silicon photonics (SiPh) based high-density co-packaged optics, optical computing, and AI, and enable a leap in performance, efficiency, cost, and bandwidth scaling compared with previous technology generations."
- "The new specifications will leverage IEEE and ITU-T standards. There is no plan to standardize link parameters as these will remain unique to applications."
- "CW-WDM MSA Technical Specifications Rev 1.0" was recently released on June 8th.

https://cw-wdm.org/

Promoter Members

Observer Members

Source: J. Johnson, "Advanced Laser Technologies in Post-100Gbaud Era", OFC 2021, Panel Th5C

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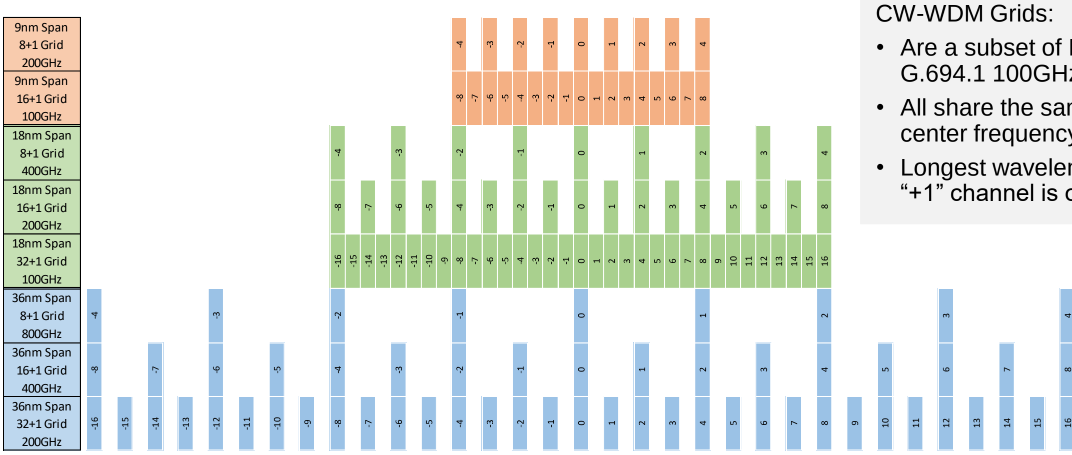
CW-WDM grid sets



Freq (THz)	WL (nm)
233.8	1282.26
233.7	1282.81
233.6	1283.36
233.5	1283.91
233.4	1284.46
233.3	1285.01
233.2	1285.56
233.1	1286.11
233.0	1286.66
232.9	1287.22
232.8	1287.77
232.7	1288.32
232.6	1288.88
232.5	1289.43
232.4	1289.98
232.3	1290.54
232.2	1291.10
232.1	1291.65
232.0	1292.21
231.9	1292.77
231.8	1293.32
231.7	1293.88
231.6	1294.44
231.5	1295.00
231.4	1295.56
231.3	1296.12
231.2	1296.68
231.1	1297.24
231.0	1297.80
230.9	1298.36
230.8	1298.93
230.7	1299.49
230.6	1300.05
230.5	1300.62
230.4	1301.18
230.3	1301.75
230.2	1302.31
230.1	1302.88
230.0	1303.45
229.9	1304.01
229.8	1304.58
229.7	1305.15
229.6	1305.72
229.5	1306.29
229.4	1306.85
229.3	1307.42
229.2	1308.00
229.1	1308.57
229.0	1309.14
228.9	1309.71
228.8	1310.28
228.7	1310.85
228.6	1311.43
228.5	1312.00
228.4	1312.58
228.3	1313.15
228.2	1313.73
228.1	1314.30
228.0	1314.88
227.9	1315.46
227.8	1316.03
227.7	1316.61
227.6	1317.19
227.5	1317.77
227.4	1318.35

CW-WDM Grids:

- Are a subset of ITU-T G.694.1 100GHz grid
- All share the same center frequency
- Longest wavelength "+1" channel is optional

https://cw-wdm.org/

Source: J. Johnson, "Advanced Laser Technologies in Post-100Gbaud Era", OFC 2021, Panel Th5C

* IEEE 802.3 400GBASE-LR8 frequencies highlighted in red

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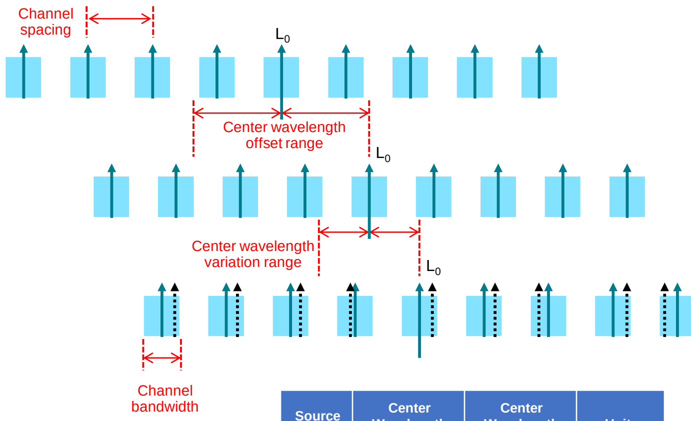
Uncooled "Flexible Wavelength" grid example

- The CW-WDM MSA spec defines "flexible wavelength" grids:
  - Center wavelength of the grid can have an initial offset of up to ±5nm from the nominal grid
  - Center wavelength can vary an additional ±2.5nm over environmental conditions, tracked by tunable ring resonator filters and modulators
  - Individual lasers must remain within the channel bandwidth relative to the offset + varying operating grid
- The flexible wavelength concept allows for efficient uncooled CW laser operation, even on narrow grid spacing, and is ideal for comb laser sources



Source Type	Center Wavelength Offset	Center Wavelength Variation	Units
Type I	± 5.0	± 2.5	nm
Type II	± 0.5	± 0.25	nm

Source: J. Johnson, "Advanced Laser Technologies in Post-100Gbaud Era", OFC 2021, Panel Th5C

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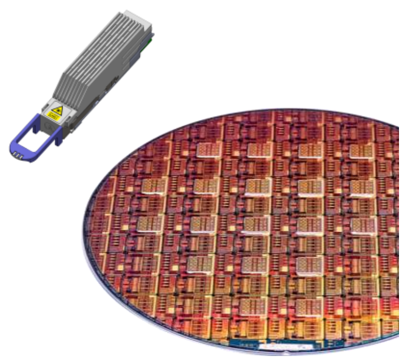
Concluding Remarks

- The rapid growth of Datacenter network connectivity represents both challenges and opportunities for co-packaged optics
- Flattening the network power consumption curve is an important aspect of managing expected growth, as well as protecting our planet
- Advanced co-packaging technologies like SiPh Chiplets in Package (SCIP) provide the highest density, most power-efficient integration of optics with switch and compute ASICs by eliminating lossy electrical interfaces
- Uncooled high power CW lasers are an essential part of achieving high networking power efficiency
- As with electrical channels, increased scale and higher end-to-end optical efficiency can be achieved through close integration of lasers and Silicon Photonic PIC to minimize optical losses



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