Considerations for Silicon Photonics Process Technologies in a Commercial Foundry Environment

Edward Preisler, Farnood Rezaie, Yasir Qamar, Minoli Pathirane, Sina Soltanmohammad, Ron Tang and Oleg Martynov

Tower Semiconductor, Newport Beach CA

edward.preisler@towersemi.com

Abstract: Aspects of silicon photonics process technologies intended for high volume production in a traditional silicon electronics-driven foundry environment are discussed. Both technological and economical challenges associated with this juxtaposition of a complex, non-standard process technology, inside of a factory geared for producing thousands of standardized electronics-based wafers per month, are described in detail.

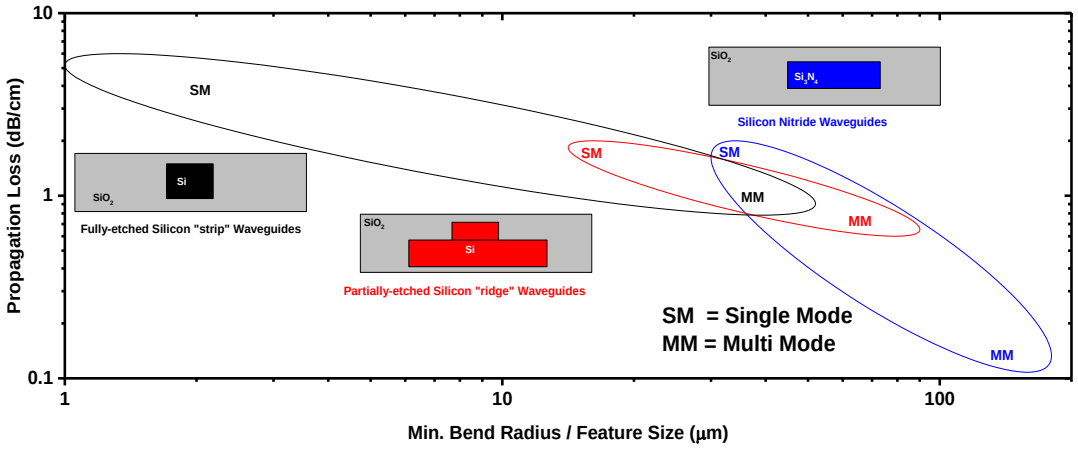
1. Introduction

Applications for silicon photonics (SiPho) process technologies have matured to the point where the volumes of silicon wafers required are large enough to require the utilization of a significant portion of the capacity available in mainstream CMOS fabs. The original promise of SiPho versus other competing technologies was always supposed to be exactly this. One can utilize the manufacturing scale and cost structure of a large silicon fab both to reduce the cost of the components and to deliver high yields for large photonics integrated circuits (PICs). However, in practice the actual implementation of high-volume manufacturing of SiPho wafers presents several challenges. Subsequent sections of this paper will discuss several aspects of a foundry SiPho process, and the technological and economic tradeoffs associated with each.

2. Passive Components

Error! Reference source not found. below shows schematically the types of waveguides (WGs) typically available in SiPho processes. The ellipses are meant to indicate the approximate ranges of propagation loss that can be achieved for each WG type on the y axis, plotted against the minimum bend radius (which can be thought of as a proxy for the minimum possible feature size) on the x axis. While all loss is parasitic and attempts are always made to minimize the overall loss in a PIC, it may be more important for a process to be able

Figure 2-1: Illustration of types of passive waveguides typically available in SiPho processes with associated propagation losses and minimum bend radii



to offer a diverse selection of WGs as shown in the figure, so that different types of WGs can be used as needed for the appropriate type of device, than just to minimize loss.

As such, while some effort should be made to reduce these losses, that effort must be weighed against the complexity and cost of manufacturing. While 193nm immersion lithography has been shown to enhance the overall performance of passive waveguide components to some degree [1] [2], these scanners are generally the most expensive tools in a fab and as such are often a bottleneck for production. Further, masks cost between 2-4x those of more economical 248nm tools.

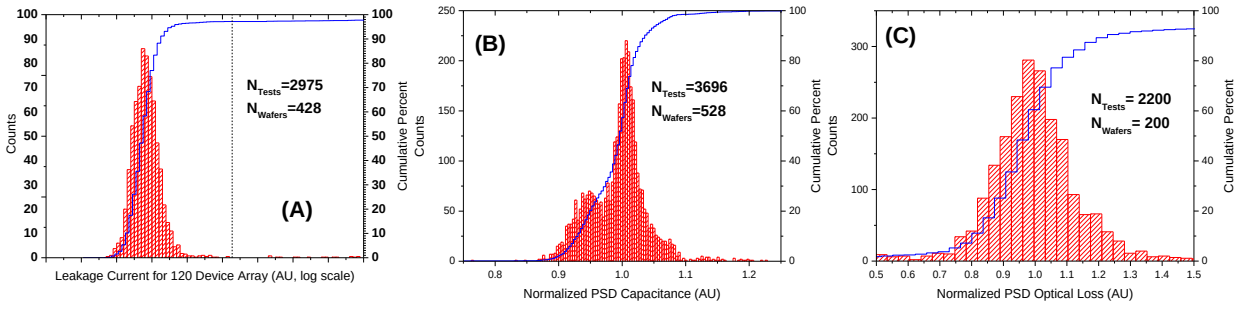
In the case of nitride waveguides, extremely low loss nitride waveguides can be obtained [3] and are very useful in use as edge couplers (EC's, see 4 below) and other passive components in traditional photonics applications as well as newer, more exotic applications [4], [5]. But to integrate these waveguides into a full SiPho process in a CMOS fab is quite challenging. Firstly, the wafer warp induced by the nitride must be compensated or somehow mitigated to be able to use advanced lithography tools to pattern the nitride. Second, to achieve very low loss, especially in the 1550nm range, hydrogen must be purged from the nitride film and surrounding cladding as much as possible which usually necessitates a large thermal cycling step which can, in turn, make integration with other devices challenging. In general, the benefit of having an integrated low-loss nitride layer in the SiPho process outweighs the process challenges.

3. Active Components

Almost all SiPho processes include a Germanium-based photodiode (PD) device for detecting the infrared light being used by the process. The basic figures of merit for the devices and corresponding tradeoffs are well understood: dark current, responsivity and RF bandwidth are all of concern to varying degrees in different kinds of PICs. While a certain minimum level of performance is required for each of these applications (see [6] for typical values for a commercial foundry process), perhaps of greater concern are the yield and reliability of these devices.

In Figure 3-1 (A) below, dark current data for arrays of 120 devices, tested on several sites each on hundreds of production wafers is shown. While efforts are made at the outset of development to optimize the device, large statistical datasets like that shown in the figure are the only real way to understand subtle changes in fab tool conditions and variations in processing that will affect product yields in volume production.

Figure 3-1: Statistical data for (A) Germanium PD Array Dark Currents, (B) PSD Capacitance and (C) PSD optical loss



Other concerns associated with the manufacturing of Ge PDs include the long cycle times required, usually on single-wafer reactor tools, to do the actual Ge growth. This can serve to make the Ge deposition step the main bottleneck for the production flow if there is not already a large installed infrastructure of reactors in the fab.

Mach Zehnder Modulators (MZMs) are the primary modulator device used in SiPho processes. The processing of the phase shifter diode (PSD) element that makes up the core element for the MZM device is simpler than that of the

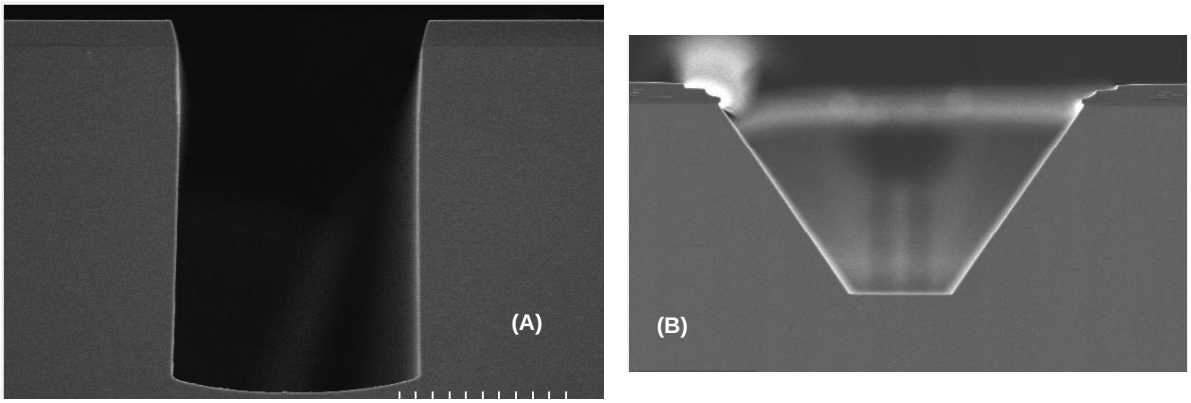
Ge PD since it only involves silicon etching and implantation steps common to CMOS processes. However, the challenge for the fab becomes controlling this intrinsically sensitive device, requiring both electrical and optical monitoring. This presents another tradeoff from the fab point of view — there is much information about optical and opto-electric devices that cannot be captured by electrical testing alone but optical testing is relatively slow and expensive compared with electrical testing. It is necessary at least to sample and measure some subset of the most important optical figures of merit for critical devices. Figure 3-1 (B) above shows example statistics for the capacitance of a PSD and Figure 3-1 (C) shows example statistics for the optical loss of a PSD, both of which must be monitored to get the full picture of the variability in a PSD in production.

4. Optical Coupling

Depending on the product configuration, either vertical incidence grating couplers (GCs), or ECs are used to allow the PIC to interact optically with the outside world. When edge coupling is possible it is often preferred because of its much wider optical bandwidth and insensitivity to polarization state as compared with GCs. To enable ECs for a PIC it is often necessary to enable "MEMS-like" processing involving deep oxide etching and deep, isotropic, or crystallographically preferential silicon etching. While these types of etch processes are not wholly unknown to CMOS fabs, they require tooling and integration schemes not common to mainstream fabs.

Figure 4-1 below shows two examples of deep oxide and silicon etching to enable ECs as part of a SiPho process offering.

Figure 4-1: Two examples of MEMS-like etch processing to enable optical edge coupling. Figure (A) shows a deep vertical silicon etch to enable placement of an optical fiber right up against the side of a die. Figure (B) shows a cross section of a "V-Groove" trench intended for passive horizontal and vertical alignment of an optical fiber.



From the fab processing point of view, these are slow and costly processing steps. But from the point view of the end-product, they can save a significant amount of cost and time in packaging. Thus, despite the cost and complexity of these modules, the effort can be justified by the cost saved by foundry customers in terms of the overall product cost.

[1] S.Y. Siew et al., "Review of Silicon Photonics Technology and Platform Development", J. Lightwave Tech. **39**, issue 13, 2021, pp. 4374-4389

[2] Selvaraja, et al., "Subnanometer Linewidth Uniformity in Silicon Nanophotonic Waveguide Devices Using CMOS Fabrication Technology", IEEE J. Sel. Topics in Quantum Electronics, **16**. 2010, pp. 316 - 324.

[3] Blumenthal et al., "Silicon Nitride in Silicon Photonics", Proc. IEEE, **106,** iss. 12, 2018, pp. 2209-2231

[4] Morin et al., "CMOS-Foundry-Based Blue and Violet Photonics", Optica 8, Iss. 5, 2021, pp. 755-756.

[5] El Dirani et al., "Ultralow-Loss Tightly Confining Si_3N_4 Waveguides and High-Q Microresonators", Optics Express **27**, iss. 21, 2019, pp. 30726-30740.

[6] Zhu et al., "A High Performance Ge PIN Photodiode Compatible with High Volume Silicon Photonics Production Processes", IEEE Int. Conf. Group IV Photonics, 2018.