Energy efficient OEO conversion and its applications to photonic integrated systems

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Abstract: We describe nanophotonics-based opto-electric devices and their femtofarad integration. The combination of these devices and optical interference units has a potential to provide energy-efficient and ultra-low latency optical information processing. © 2021 The Author(s)

1. Introduction

Many arithmetic devices based on electronic circuit technology are used in current information processing, and further improvement in performance is required from the viewpoint of latency and the energy consumption. To meet these demands, we are working toward the development of information-processing chips that use light. For example, complementary metal-oxide semiconductor (CMOS) processors improve throughput by integrating a huge number of nanometer-sized transistors into a chip at ultra-high density, holding a large amount of information in it, and processing the information in parallel. CMOS technology is the most useful technology in this regard. However, light can transmit information at the speed of light without being subject to electrical constraints (RC delay due to capacitance C and resistance R) during the signal-propagation process. Therefore, photonic devices far outperform electronic devices in terms of wideband and low latency. Combining these electrical and optical advantages requires innovative technology that significantly reduces overheads such as energy, processing time, and system load during electrical-to-optical (E-O) and optical-to-electrical (O-E) signal conversions. In this talk, we will review our E-O and O-E converters using nanophotonics and silicon photonics and discuss their potential in integrated-photonics-electronics-convergence system.

2. Opto-electronic devices for seamless interface between CMOS and photonic layers

In today's computers, the typical ratio of data-transfer rate (Byte/s) to floating point operations (Flops) is about 0.1–0.5 B/F. This means that about 100 calculations can be executed while one piece of data is being transferred from memory, that is current memory access is very slow compared with processor speed. Therefore, various on-chip optical interconnects targeting B/F = 1 by using silicon photonics (SiPh) technology are being actively pursued [1]. However, to keep up with the progress in computing performance while maintaining this ratio, it is necessary to increase the I/O-bandwidth density (bit/s/mm^2). To do this, we need to not only drive the device faster but also reduce the size of the device. In addition, to reduce the input power density to about 100 W/cm^2, energy costs need to be further reduced.

To meet these requirements, we are focusing on photonic crystals (PhCs). PhC is a structure in which air holes are arranged on a semiconductor substrate at a period of about the wavelength of light, as shown in Fig. 1. This is a technology that enables wavelength-sized optical confinement and reduces the size of optical devices and their energy consumption by several orders of magnitude compared with conventional ones. We previously developed a buried-hetero structure to embed a wavelength-sized active medium in a nanocavity consisting of a PhC and succeeded in fabricating PhC-based E-O and O-E devices, i.e., a laser diode (LD) [2], electro-optic modulator (EOM) [3] and photodetector (PD) [4,5]. They can operate at a very low

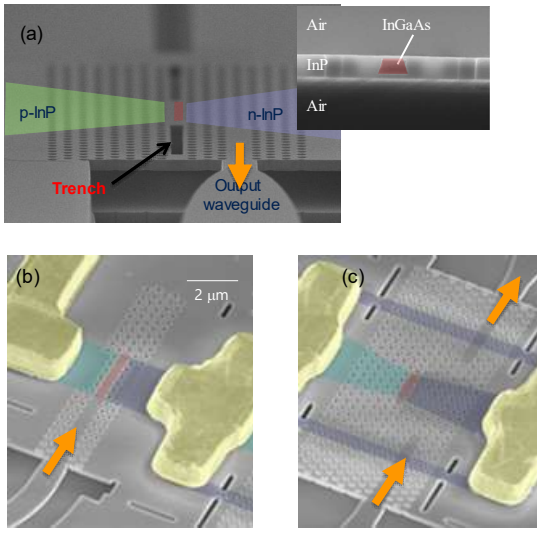

Fig. 1 PhC-based devices using buried-hetero structure (a) LD, (b) PD, (c) EOM

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energy cost of about fJ/bit. These basic devices are attracting attention as key devices for eliminating input/output (I/O) bottlenecks in information processing.

The largest advantage of PhC-based devices is their small size and small capacitance. For example, SiPh-based PDs have a large capacitance due to their size. Therefore, to drive the receiver circuit at high speed, it is necessary to convert the photocurrent generated by the PD into a voltage with a transimpedance amplifier (TIA) and input it to the complementary metal-oxide semiconductor (CMOS) circuit. Since the capacitance of our PhC-based device is very small, high-speed driving is possible while minimizing the RC delay even if current-voltage conversion is carried out using only the loaded resistance without a TIA. Because of its high sensitivity, it is not necessary to apply the reverse bias required for conventional PDs, and it is possible to significantly reduce energy costs. As a result, our PhC-based PD eliminates the need for large power-hungry electronic circuits such as TIAs, can be small, i.e., 50 μm2 for one device, incur low energy cost of <10 fJ/bit, and execute high-speed operation of 10 Gbit/s. These correspond to 200 Tbit/s/mm^2 and 200 W/cm^2, which means that our PhC-based device has the potential to achieve 10 times the I/O-bandwidth density of a SiPh-based device while suppressing the input power to I/O.

3. Electro-optic device for direct conversion from electrical digital signals to optical analog signals

Next, we discuss the slightly more sophisticated E-O component that mediate between CMOS circuits and optical interference units (OIUs). The use of light not only for communication but also for computation was actively studied in the 1980s and has been attracting attention again with the progress in nanophotonics. An OIU makes it possible to execute binary decision diagram based operations [6] and multiply-accumulate operations (MAC) [7,8] in the photonic domain by using light transmission and interference in the optical network. Basically, light is only propagated to the optical network, so the smaller the device, the lower the operation latency. Energy is also not consumed by propagating optical signals. For example, SiPh is said to be an order of magnitude more efficient than state-of-the-art CMOS circuits in terms of both computational efficiency (MACs/s/mm^2) and energy efficiency (MACs/J) [8], and smaller nanophotonics further improve performance. Basically, light is treated as an analog signal in an OIU, so to effectively use the ultra-low latency of an OIU, the conversion overhead from electrical digital to optical analog that occurs between the CMOS circuit and OIU must be reduced as much as possible.

It is common to input an electrical analog signal to E-O devices in an optical circuit through an electrical digital-to-analog converter (DAC), but this increases latency and power consumption. To reduce the conversion overhead, several types of electro-optical DACs (EO-DACs) have been proposed that directly convert an electro-digital signal into an optical analog signal. However, the insertion loss of a conventional EO DAC weighted by loss increases as the number of input bit (N) increases. An EO-DAC weighted by branching [9] can reduce the loss but the asymmetric coupler causes wavelength dependence. An EO-DAC using segmented phase shifters [10] is known as almost lossless. However, since E-O phase modulators (PMs) are serially connected in the propagation direction of the optical signal, electrical noise derived from N PMs accumulates.

Therefore, we developed a circuit topology (CT) EO-DAC [11] weighted by symmetric Y branches. The circuit configuration of EO-DAC is shown in Fig. 2(a). First, the input light is branched into N waveguides. A PM is inserted in each of the N waveguides, and digital electric bit signals from least significant bit (LSB) to most significant bit (MSB) are input to N PMs. When the digital input value is "0" ("1"), the phase is modulated so that the output phase is π (0). Finally, a binary phase-shift keying (BPSK) signal can be obtained after the phase-modulated lights are combined. With our CT EO-DAC the loss gradually approaches zero as N increases as shown in Fig. 2(b). Moreover, the number of PMs in the signal-propagation direction is only one, so noise accumulation can be avoided. To the best of our knowledge, only our EO-DAC can achieve both low loss and low noise, resulting in the highest signal-to-noise ratio ever obtained, resulting in high-resolution operation.

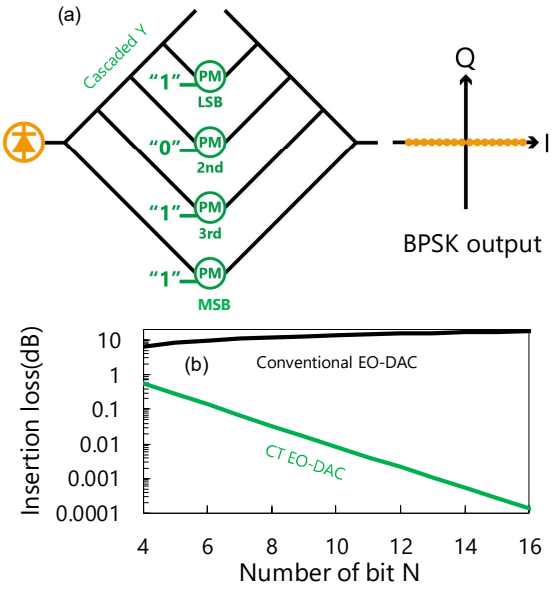

Fig. 2 CT EO-DAC (a) circuit configuration of CT EO-DAC. (b) Comparison of the insertion losses between the conventional EO-DAC and CT EO-DAC

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4. Optic-electro-optic converter for non-linear operation in optical circuit

Finally, we discuss the E-O and O-E components between OIUs. The largest advantage of an OIU is that MAC can be executed by linear phenomena such as light transmission and interference. However, complex signal processing cannot be executed without non-linear processing. In addition, OIUs do not have the ability to recover signal strength, so optical loss limits the scale of the circuit. Therefore, functions such as optical signal control by optical signals, neuron-threshold processing and signal amplification are indispensable between OIUs, but it is not realistic to adopt conventional optical non-linear elements from the viewpoint of size and energy consumption. Although it is possible to impose non-linear processing on electronic circuits, if this process is executed frequently during operation, the power consumption and delays in E-O and O-E conversions can become a bottleneck. An optic-electro-optic (O-E-O) device [12] that integrates a PD and EOM should be a means to solve such problems. However, current O-E-O devices are large with a capacitance of > 100 fF, require light energy of 100 fJ/bit or more, and the bandwidth limitation by RC becomes a bottleneck.

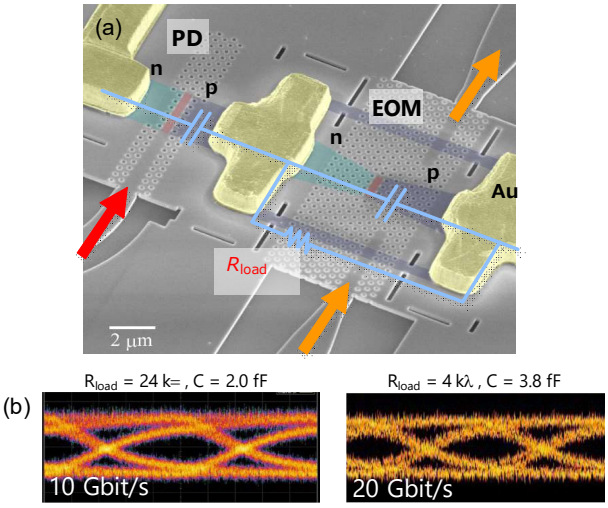

Fig. 3. O-E-O converter by the combination of low-capacitance PD and EOM.

Therefore, we developed an O-E-O convertor that closely integrates a nanophotonic PD and EOM based on PhCs [3], as shown in Fig. 3. The photocurrent generated from the PD by the input optical signal is converted to a voltage through the load resistor (R_{load}), which modulates another optical signal input to the EOM. The light energy required for the PD is very small, i.e., 1.6 fJ/bit. Since the capacitance is estimated to be 2 fF, even if the conversion voltage is increased using a high-load resistor of 10 kΩ or more, high-speed drive of 10 Gbit/s or more is possible. An optical signal gain of approximately 3 dB has been observed, which also functions as an optical repeater. In addition, the optimal combination of OIUs and O-E-O devices can exponentially reduce the power used for calculations [6]. Since our O-E-O device can introduce electronic non-linearity in a region very close to an optical signal with energy saving, space saving, and low latency, it should be indispensable for high functionality of ultra-low latency operation using OIUs.

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5. References

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