Optical Damage Threshold Screening Methodology for 28 GBd, Long Wavelength Avalanche Photodiodes

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Abstract: We present a novel scalable wafer screening method that guarantees an optical damage threshold larger than +5 dBm for 28 GBd long wavelength avalanche photodiodes over large-scale production volumes. © 2022 The Author(s)

1. Introduction

Over the last two decades, global network traffic has experienced an exponential growth. This trend is expected to continue in the future, driven by the ever-increasing demand for data-centric applications and the mass adoption of faster networks such as fiber-to-the-home or 5G mobile services [1, 2]. Most of this data travels over fiber optics networks, fueling a large demand for faster and more efficient optoelectronic devices. Avalanche photodiodes (APDs) are a key technology in this field, enabling higher sensitivity receivers for extended network reach.

Despite being optimized for low-power optical signals (~10^{-6} W), most practical applications of APDs require a large dynamic range to ensure operation up to overload conditions (10^{-4} - 10^{-3} W). Therefore, APDs should also be able to withstand high optical input powers, i.e. they should have a high optical damage threshold (ODT). A simple way to protect APDs from optical damage is to use a passive quenching resistance (R_s) in the biasing path (i.e. in series with the APD, see Fig. 1a). Under strong optical illumination, the large photocurrent generated by the APD flows through the resistor, causing a reduction of the effective APD voltage (V_{APD}) with respect to the applied bias voltage V_r:

$$V_{APD} = V_r - R_s I_{ph}$$

This voltage drop reduces the avalanche gain, therefore decreasing the photocurrent and protecting the device from optically-induced overcurrent. However, if this causes V_{APD} to drop below the APD turn-on voltage (V_{on}), the device will effectively shut itself down, causing a steep increase in the observed bit error rate (BER) and a collapse of the bandwidth. Therefore, the selection of R_s is constrained by two requirements: (1) it should be small enough so that $V_r - R_s I_{ph} > V_{on}$ even at high optical input power; (2) it should be large enough to keep the photocurrent at high optical input power below the current density limit of the APD material. These two conflicting requirements have made obtaining high-speed APDs with elevated ODT a challenge [3].

To overcome this bottleneck, we developed a wafer-level screening methodology that guarantees both overload performance and high ODT levels on 100% of the devices at industrial volume production. The procedure is validated by sample testing at different temperatures, demonstrating the resilience of the APDs to high optical input power over the full operating temperature range, from -40 °C to +90 °C.

2. Wafer Level Screening Methodology

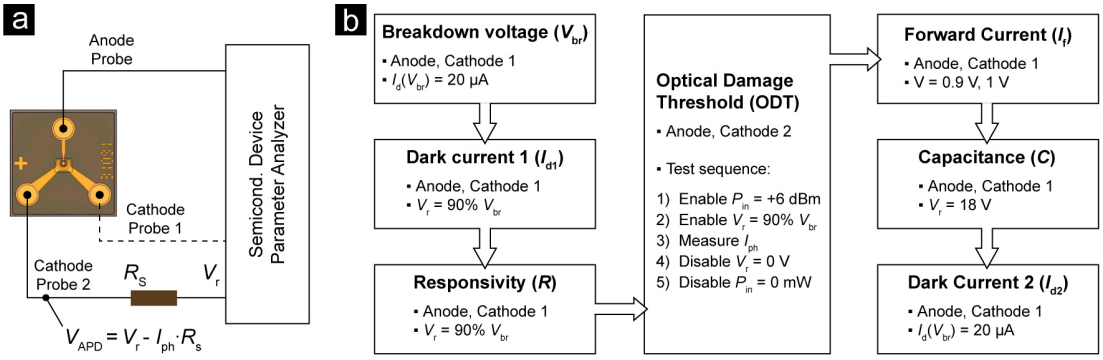

Fig. 1. a) Device contacting scheme on the wafer probe station. b) Flow chart of the wafer testing procedure.

The wafer-level screening is performed using a fully automated wafer probe station. The APD wafer is placed on a transparent chuck which allows back-side illumination, while the device is contacted from the top-side with three probe needles (anode, cathode #1 and cathode #2). All measurements are performed using a Keysight B1500A Semiconductor Device Parameter Analyzer. The whole testing procedure is shown in Fig. 1.

First, cathode probe #1 is used in combination with the anode probe to measure the fundamental characteristics of each APD chip: breakdown voltage (V_{br}), dark current at 90% V_{br} (I_d) and responsivity (R) at -20 dBm optical input power. After this, the ODT test is started, this time using the anode probe in combination with cathode probe #2, which contains a quenching resistor R_s = 8 kΩ (see Fig.1a). During the ODT test the APD is first illuminated with a +6 dBm optical input, and then biased at 90% V_{br} while recording its photocurrent. Then, a second series of measurements is performed, including capacitance (C), forward current (I_f) and another dark current measurement (I_{d2}). The I_{d2} value is used to identify optically-induced damage. APD chips showing elevated dark current after optical stress (exceeding the device specifications) are defined as failed and discarded.

3. Wafer Screening Validation

To validate the screening procedure, sample APD chips which passed the wafer screening test were mounted in a hermetically sealed TO-46 package (DUT) for detailed measurements. The DUTs are placed in a climate chamber and connected according to the schematics in Fig. 2a. The DUTs are then tested at different temperatures between -40°C and +90°C using a R_s = 9 kΩ series resistance. Two types of tests are performed: a sweep of the optical input power at constant bias, and a sweep of the bias at constant optical input power.

The first test consists of ramping up the optical input power from P_{in} = -20 dBm to P_{in} = +6 dBm (see Fig. 2b) under a fixed reverse bias V_r = 90% V_{br}. As can be seen in Fig.2b, the photocurrent I_{ph} increases with the applied optical input power. Above P_{in} ~ -2 dBm, the photo-response starts to flatten, since V_{APD} is close to the turn-on voltage (V_{on}). In this regime, any optical input power increase produces a further reduction of the effective APD voltage, thus reducing its gain and in turn limiting the photocurrent. Therefore, the APD remains in this stable operating condition.

The second test is a sweep of the bias voltage V_r from 0 V to 90% V_{br} under a fixed optical input power P_{in} = +6 dBm. As shown in Fig. 2c, the photocurrent I_{ph} increases with the bias voltage V_r. No failures were detected in either test.

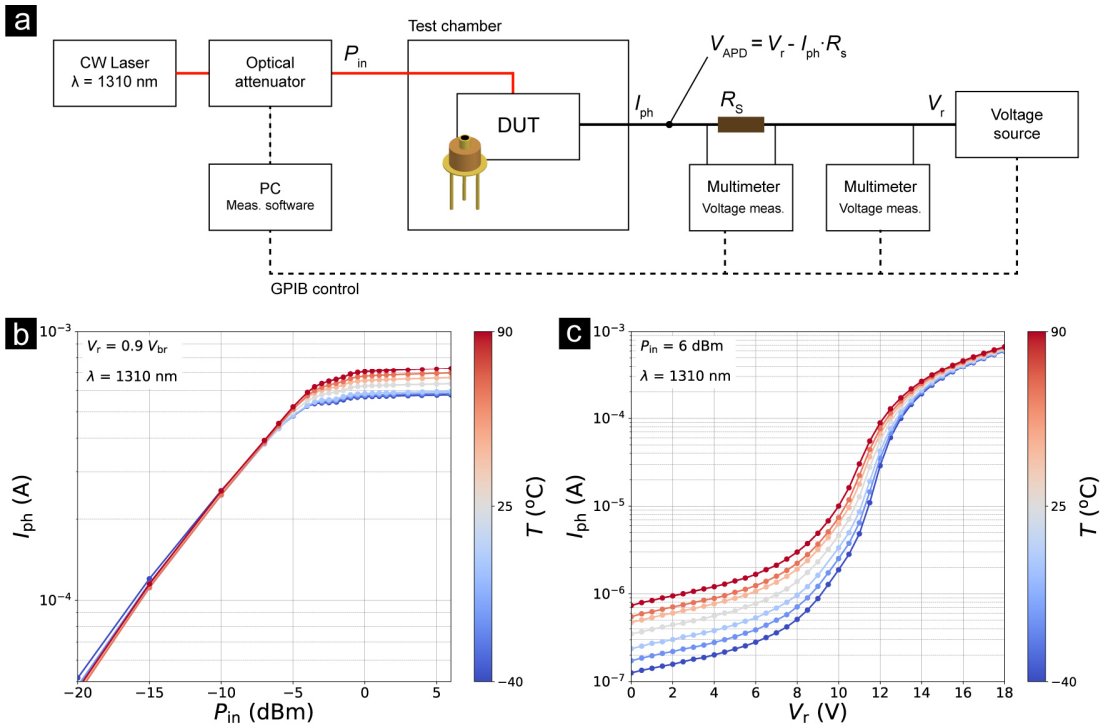

Fig. 2. a) Schematic of the test setup. b) Photocurrent I_{ph} vs. optical input power P_{in} at different temperatures for V_r = 90% V_{br}. c) Photocurrent I_{ph} vs. reverse bias voltage V_r for an optical input power P_{in} = +6 dBm at different temperatures. In both cases a series resistor R_s = 9 kΩ is used.

Table 1. Test results

Parameter	Symbol	Unit	-40 °C	25 °C	90 °C	SS
Breakdown Voltage at I_d = 20uA	V_{br}	V	19.38 ± 0.02	20.02 ± 0.02	20.61 ± 0.02	6
Dark Current at 90% V_{br}	I_d	nA	2.3 ± 0.1	11 ± 3	100 ± 17	6
Responsivity at 90% V_{br}	R	A/W	4.6 ± 0.2	4.6 ± 0.2	4.6 ± 0.2	6
ODT power ramping V_{APD} = 90% V_{br}	ODT_P	dBm	≥ 6	≥ 6	≥ 6	6
ODT voltage ramping	ODT_V	dBm	≥ 6	≥ 6	≥ 6	6

Table 1 summarizes the test results, including the temperature dependence of breakdown voltage (V_{br}), dark current (I_d) and responsivity (R) of the DUTs. The sample size SS = 6. The ODT is defined as the highest optical input power tested which does not damage the device.

The APDs were also tested for their frequency response to ensure that the chosen R_s is compatible with operating under overload conditions. Fig. 3a shows the bandwidth as a function of optical input power at the operating reverse bias voltage V_r = 90% V_{br} for R_s = 9 kΩ. The bandwidth remains stable up to an overload condition of P_{in} = -3 dBm. Fig. 3b shows the sensitivity of an APD ROSA prototype with a commercially available transimpedance amplifier (TIA). The BER was determined by measuring the Q-factor with an Agilent 86100C oscilloscope. As shown in the plot, for P_{in} = -21 dBm the BER is better than 1e-12, and a BER of 5e-5 can be achieved at less than P_{in} ~ -27 dBm.

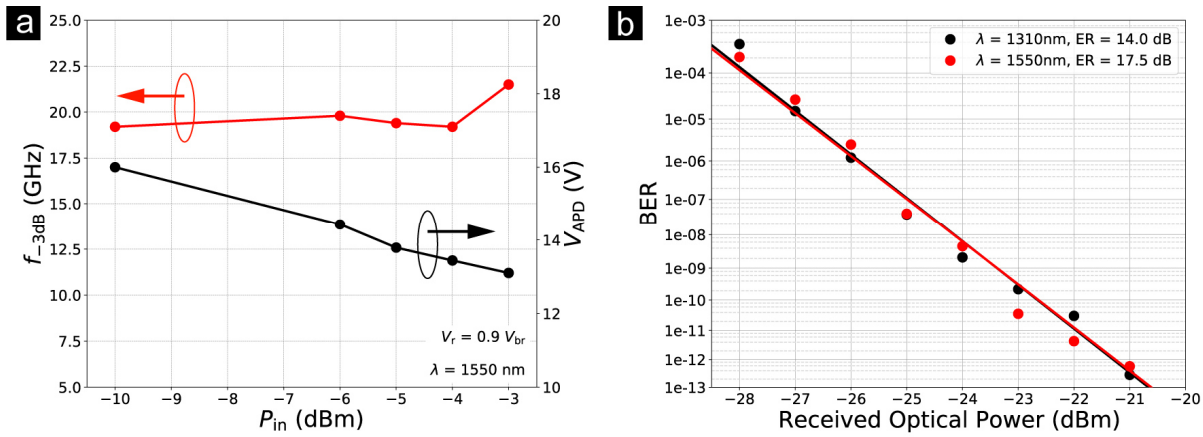

Fig. 3. a) APD -3dB bandwidth f_{-3dB} (left axis) and APD voltage V_{APD} (right axis) vs. optical input power P_{in} for R_s = 9 kΩ and V_r = 90% V_{br}. b) APD ROSA sensitivity measurements at 25Gbps for λ = 1310, 1550 nm.

4. Conclusion

We developed a methodology for full-wafer screening against optical damage that is compatible with large volume production. The technique is validated on high-speed avalanche photodiodes, guaranteeing an optical damage threshold of at least +5 dBm with a protective series resistance of R_s = 9 kΩ.

5. References

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[2] World Bank 2021, "World Development Report 2021: Data for Better Lives", Washington DC: World Bank.

[3] J. J. S. Huang, H. S. Chang, and Y. H. Jan, "Reliability Scaling of Nanoscale Avalanche Photodiodes in High-Speed Optical Communication.", Applied Physics Research **11.6** (2019).