Optical Binary Switched Delay Line based on Low Loss Multimode Waveguide

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Abstract: We demonstrate low loss, 7-bit, switched delay line, with 6.4 ns measured delay span. The geometrically-optimized delay lines achieve 3.3 dB/m (0.25 dB/ns) measured loss. The design is fabricated in a commercial silicon photonics process. © 2022 The Author(s)
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1. Introduction

Low-loss waveguides are key enablers in photonic integrated circuits and systems including those for communications, computation, sensing, and microwave signal processing [1-3]. The loss is particularly important in signal processing applications where a large delay is needed. In this case, waveguides with larger core size may be used to enhance the confinement and reduce the interaction of the optical field with the sidewall roughness to reduce loss. Such waveguides naturally support multiple propagating modes. This leads to large losses at any discontinuity in the waveguide geometry including waveguide bends. Therefore, most of the existing large delay lines use spiral structures with very large bends (few mm) to solve this issue [3-6]. The main drawback of this approach is the inability to realize large delay lines in a compact formfactor. In this work, we use tapered waveguides to connect the low-loss multi-mode wide-core straights waveguides to single-mode compact waveguide bends that leverage geometrically optimized Euler shapes to reduce their loss.

Variable delay line is a key enabler in many RF photonic applications such as microwave filtering, correlators, and self-interference cancelations [6-7]. In this work, we demonstrate a switched delay line structure leveraging the aforementioned low-loss compact delay lines and 2x2 Mach-Zehnder Interferometer (MZI) switches.

2. Low-Loss Delay Line

This work realizes low-loss optical delay lines that are laid out in a meandered way with three enabling features (Fig. 1a). The 4.5-mm-long straight regions of the structure are realized as 3-μm-wide multimode waveguides (MM-WG), spaced with 5 μm pitch. The length of this straight waveguide is limited by the available die size (5 mm x 5 mm). The lower limit for the spacing between the adjacent waveguides is determined by the power coupling and the

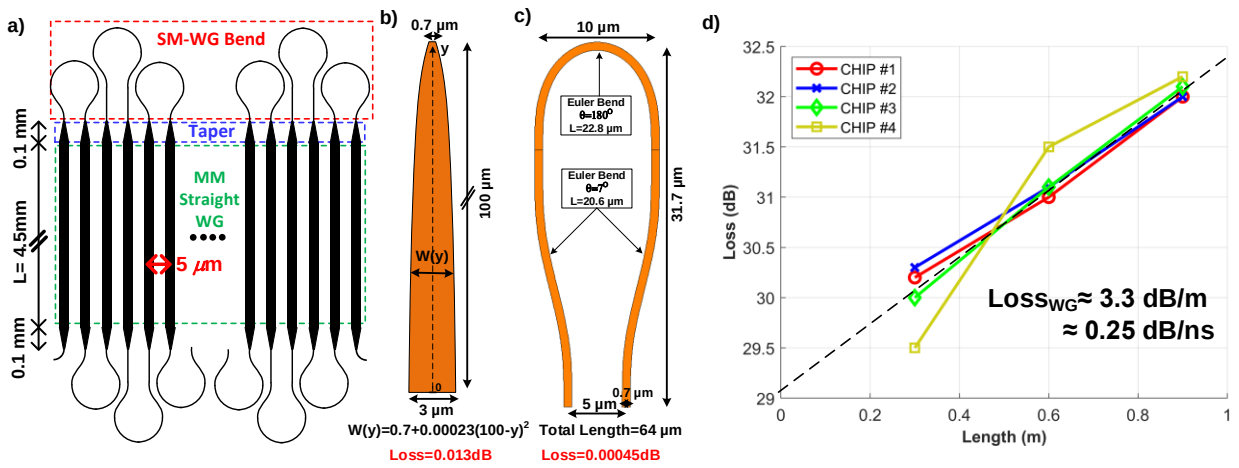

Fig. 1. (a) Proposed geometry of the low-los silicon photonics delay line. (b) Detailed geometry of the single mode to multimode waveguide taper along with the FDTD loss simulation results. (c) Detailed geometry of the 180° clothoid bend along with the FDTD loss simulation results. (d) Measured loss of the delay line across four different chips using the cut-back technique showing direct loss of three different delay lines lengths (0.3 m, 0.6 m, 0.9 m) in addition to the estimated loss of the straight multimode wide waveguide per unit length and delay.

loss of the tighter U-turn bend. In our implementation, the latter is the limiting factor as the power coupling between two wide-core waveguides with high confinement is very small (less than 30 dB based on the even-odd mode simulation across 4.5 mm). At the two ends of the straight region, 0.1-mm-long waveguide tapers are used to narrow the waveguide width to 0.7 µm to obtain a single-mode waveguide (SM-WG). A parabolic shape taper, as shown in Fig. 1b, has been used to obtain a smaller loss compared to the regular linear shape tapers [8-9]. The waveguide U-turns that connect two adjacent straight waveguides with 5 µm spacing use such 0.7 µm single-mode waveguide regions with an Euler geometry [10-11] to lower the loss. To reduce the loss, we use two smoothly changing (7°) bends leading to a 5-µm-radius 180° bend. The detailed geometry is shown in Fig. 1c. The U-turn section is wider than the waveguide pitch, thus an interleaved layout is used as shown in Fig. 1a. The proposed delay line structure was fabricated using PH18MA Tower Semiconductor Silicon Photonics (SiP) process. A cut-back method was intended to measure the loss of the delay line and the U-turn bends. Three different structures were designed with different total straight MM-WG lengths (0.3 m, 0.6 m, and 0.9 m), by changing only the length of the straight MM-WG and keep the same number of bends (585). Figure 1d, shows the measured optical loss values with respect to a reference structure (two grating couplers connect back-to-back). From the slope we can get the loss of the MM-WG to be 3.3 dB/m or with respect to the introduced delay it is equivalent to 0.25 dB/ns. From the zero-length structure we can get the loss of the bends, it is equal to 0.048 dB per U-turn (two tapers and one 180° bend). Given the maximum die size (5 mm), we need around 19 bends to implement 1 ns of delay corresponding to 0.91 dB of loss. The total loss after adding the 1 ns MM-WG length (0.25 dB) is around 1.16 dB. This number can be reduced accordingly be using larger die sizes to reduce the number of the U-turns bends or by further improving the design of the U-turn bends. The proposed delay line design is very area efficient, per unit delay it consumes 0.5 mm^2/ns.

3. Variable Binary-Coded Delay Line

We used the same technology TowerJazz (PH18MA) to demonstrate a digital variable delay line system using the delay line structures that is described in the previous section. The structure, shown in Fig. 2a, consists of seven cascaded parallel paths one has delay line structure and one with zero (neglected) delay, separated by 2x2 MZI optical switches. By configuring each optical switch Bar and Cross setting we can control the total delay of the whole structure. The seven delay lines have delays values follows a binary pattern of 3.2 ns, 1.6 ns, 0.8 ns, 0.4 ns, 0.2 ns, 0.1 ns, and 0.05 ns. The binary pattern is achieved by halving the number (N) of the straight waveguides (L= 4.5 mm) used in the following delay line section except for the two least significant bits (LSBs) where the length of

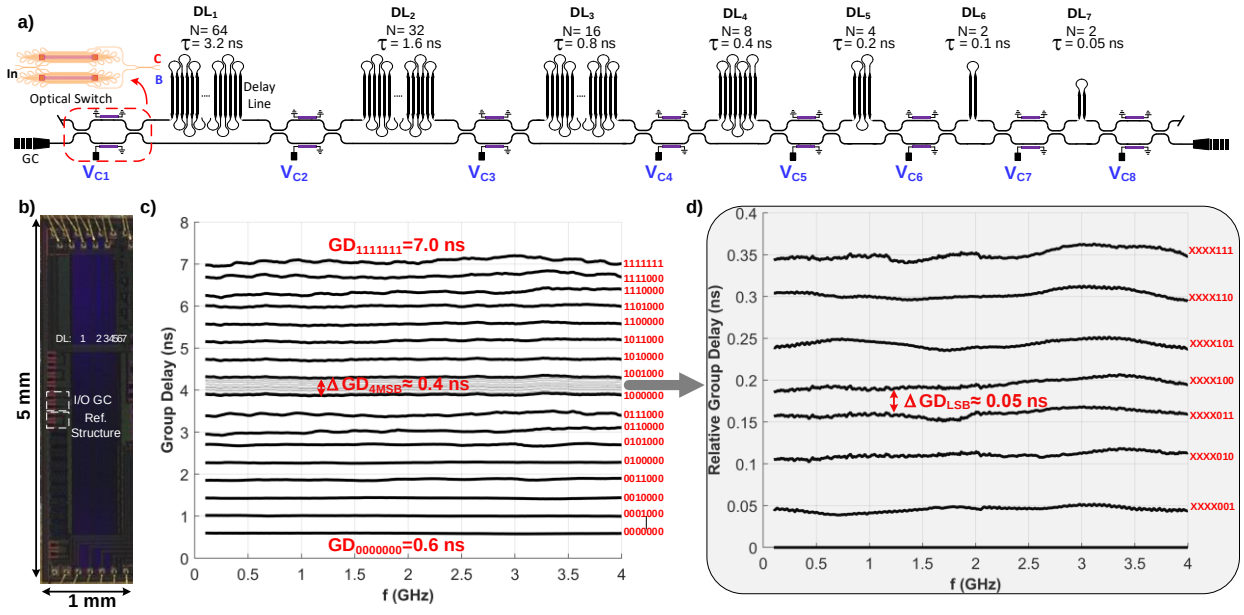

Fig. 2. (a) Schematic Diagram of the proposed variable switched optical delay line, showing the number of waveguides (N) and delay (τ) of each delay line section and the low loss optical switch layout design (b) Microphotograph of the fabricated structure showing the location of each delay line section. (c) The group delay measurements of the proposed structure versus the frequency of the modulated RF signals around the optical carrier, showing the minimum and maximum delays and all the coarse tuning 4 MSBs (DL1-DL4) configurations' delays (d) The measured relative group delays of the fine tuning 3 LSBs (DL5-DL7) configurations.

the straight waveguide is halved while using the same number of waveguides (N=2). The corresponding loss of each delay line section is 3.83 dB, 1.89 dB, 0.92 dB, 0.44 dB, 0.2 dB, 0.08 dB, and 0.06 dB, respectively. The optical switch layout is also shown in Fig. 2a. For the phase shifter element, we used a geometrically-optimized, heat-reuse, thermo-optic phase modulator structure (design B in [12]) to achieve low power consumption and low loss. One phase shifter is used to introduce the required phase difference between the two arms and the other one is just dummy connected to equalize the loss between the two paths. The measured P_π and loss of the phase shifter are 2.5 mW and 1 dB, respectively. As expected, the measured switching power to switch the laser from one port to the other is equal to the P_π of the phase shifter (2.5 mW). The estimated loss of the optical switch is around 1 dB as the phase shifter loss dominates over the losses of the two directional couplers. The coupling between the output ports is -18 dB when the switch is in the Bar state and -30 dB when it is in the Cross state. A microphotograph image of the fabricated system is shown in Fig. 2b, showing a total area of 5 mm x 1 mm. To measure the delay of the different binary configurations of the variable delay line system, we measure the group delay of electrical RF signal passes through the system. We used an external bench-top modulator and optical receiver (photodiode and TIA) to modulate and extract the RF electrical info. A Vector Network Analyzer (VNA) was used to measure the phase of S21 from which the group delay can be extracted. It is important to mention that all the delay measurements are referenced to a zero-delay line (two grating couplers connected back-to-back) on the chip. Thus, the group delay of the other components of the testbench are automatically de-embedded. Figure 2c shows the measured delay of the system highlighting the maximum delay, the minimum delay, and the delays of the 16 binary coarse-tuning configurations of the 4 most significant bits. A zoomed measurements results of the delay of the 8 binary fine-tuning configurations of the 3 least significant bits are shown in Fig. 2d. The minimum delay is 0.6 ns, that is correspond to the delay of the optical switches and the routing. The maximum delay when the light passes in all the delay lines is 7 ns, that leads to delay span of 6.4 ns and average delay step of 0.5 ps. This structure has a minimum 8 dB loss at the 0.6 ns delay configuration (0000000) because to the eight cascaded optical switches. The loss of the maximum delay of 7 ns (1111111 configuration) is 15.3 dB. This loss can be further reduced by optimizing the design of 2x2 MZI optical switches.

4. Conclusion

Firstly, we demonstrate a low loss, area efficient, optical delay line using wide straight waveguides and low loss tapers to convert to single mode waveguides where geometrically-optimized bends are used. The measured loss is 0.25 dB/ns of straight waveguide delay and total loss of 1.16 dB including the bends losses. Secondly, this low loss delay line is used in a switched delay line binary scheme to obtain a variable delay line. The design has a tunable range of 6.4 ns with 0.05 ns resolution, and maximum loss of 15.3 dB for the largest delay of which around 8 dB is due to the 8 2x2 MZI optical switches

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