High Speed Ge/Si Avalanche Photodiode with High Sensitivity for 50Gbit/s and 100Gbit/s Optical Access Systems

Chingyin Hong[†] , Bin Shi[†] , Fan Qi, Pengfei Cai, Yanhui Duan, Guanghui Hou, Tzungi Su, Tehuang Chiu, Su Li, Wang Chen and Dong Pan*

SiFotonics Technologies Co., Ltd., 400 Trade Center, Suite 4950, Woburn, MA 01801, USA,
**Corresponding author: dp7u@sifotonics.com*

Abstract: 25GBaud and 50GBaud APDs with high sensitivity gain compared with PDs are reviewed. The great consistency and excellent performance of the APDs could great satisfy the requirements of 50Gbit/s and 100Gbit/s optical access systems, such as 400GbE datacenters, 100G ER1 and 50G PON etc.

OCIS codes: (040.1345) Avalanche photodiodes (APD); (060.4510) Optical communications

1. Introduction

The rapid increase of communication networks has led to many new services [1]. To accommodate this increase, transmission capacity of optical access systems has steadily increased over past several decades. In optical access systems, transmission capacity increasing always has a tradeoff relationship with allowable transmission distance. However, datacenters need taking into account both capacity increasing and building scale increasing at the same time nowadays. For example, hyperscale datacenters are now facing the speed transition from 100GbE to 400GbE, while scale is growing from one single building to large campus including interconnected datacenters over several to tens of kilometers. This will bring great challenges to the new generation optical access systems.

PD and APD chip are two core components for receiver side to realize a high-speed fiber optical link. Especially, APD chip can provide several dB more sensitivity improvement than ordinary PD chip due to its internal avalanche mechanism. This sensitivity gain means a tens of kilometer transmission distance extension just by a chip substitution, so APD chips are widely used in long distance fiber transmission and tense link budget applications, such as ER and PON access scenarios.

In recently discussed 400GbE standards, 8x50Gbit/s PAM4 and 4x100Gbit/s PAM4 schemes are two most attractive solutions [2]. As a multi-level modulation format, PAM4 scheme has better bandwidth efficiency and only needs half channels compared with NRZ scheme, but linearity becomes a requirement on optical devices like DFB/EML and PD/APD. This means high sensitivity 25GBaud and 50GBaud APDs with better linearity are indispensable in 25GB and 50GB PAM4 applications.

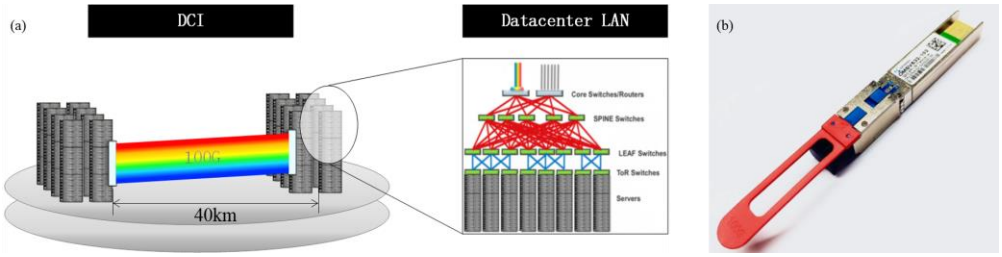


Fig. 1. (a) Schematic of datacenter interconnection. (b) SiFotonics 100G ER1 module [3].

Recently, a new standard of 100Gbit/s PAM4 ER1 transceiver was developed by 100G lambda MSA [3]. It uses high bandwidth optical components to realize 40km single channel 100Gbit/s optical transmission, which is a cost effective long distance solution like datacenter interconnection (DCI), as shown in Fig 1. This MSA needs Rx sensitivity at BER=2.4E-4 to be -14.0dBm, which means only APD component with both high gain and sufficient bandwidth can meet this specification.

Another high-volume potential application for 25GBaud and 50GBaud APDs are 25G/50G PON using NRZ formats, where only APD can meet the tense link budget. 25G/50G PON might be adopted by many countries as a direct upgrade from current 2.5G PON.

In the past several years, we have reported a series of high speed Ge/Si APD chips [4,5]. These chips exhibit high responsivity and excellent sensitivity, due to the higher gain-bandwidth product, lower ionization coefficient ratio and lower multiplication noise of silicon material. In this paper, we reviewed the DC parameters, RF characteristics and sensitivity performance of our 25GBaud and 50GBaud APD chips, which can provide strong support to applications in 400GbE datacenters, 100G ER1, and 50G PON, etc.

2. Chip structure and fabrication

The APD chips adopt a typical separate-charge-absorption-multiplication (SCAM) structure, and the whole process is completed in a standard CMOS commercial foundry. CMOS processes have been proved to be a very good APD chip manufacture platform to provide higher specification uniformity and total yield [6]. Chips in the wafer show a great uniformity, such as breakdown voltage, dark current and responsivity etc.

3. 25GBaud APD Chips

Fig. 2(a) shows the photograph of the APD chip. Both P pad and N pad are on top side, and top-illumination make the chip easy to be assembled. Typical DC measurement results are shown in Fig. 2(b). The breakdown voltage (V_{BR}), defined as the applied voltage leading to 100μA room temperature dark current, is about 19.9V. The dark current of the APD chip at V_{BR}–1V is about 0.97μA at 25ºC. The responsivity of 1310nm is 6.6A/W at V_{BR}–1V, with primary responsivity estimated to be ~0.79A/W. The typical capacitance of 25GBaud APD is 63fF.

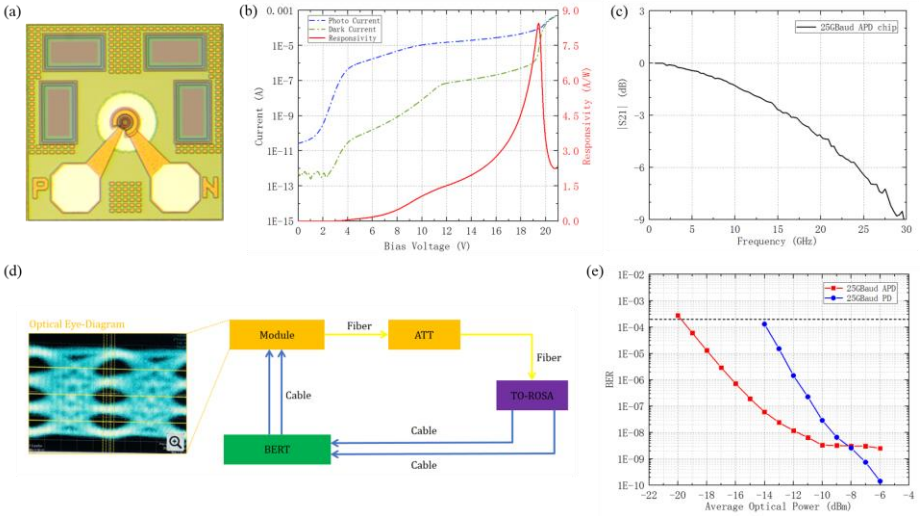


Fig. 2. (a) Optical image of 25GBaud APD chip. (b) Photo current, dark current and responsivity curves of 25GBaud APD Chip at 25ºC. (c) RF response of the APD chip. (d) Testing setup and optical eye-diagram of the light source. (e) 50Gbit/s PAM4 BER measurements in a back-to-back configuration for 25GBaud APD ROSA and PD ROSA.

RF measurements are performed with a 70GHz light component analyzer (LCA), and measured S21 curve is shown in Fig. 2(c). The 3-dB bandwidth is 16.5GHz at V_{BR}–2V. To evaluate the sensitivity performance, the chips are packaged with a commercially available TIA in a TO-CAN type ROSA and the total 3-dB bandwidth is 20GHz.

50Gbit/s PAM4 sensitivity testing is performed with the setup shown in Fig. 2(d). Inset shows the optical eye-diagram of the light source, with TDECQ=1.4dB and outer ER=5.7dB. The measured back-to-back 50Gbit/s PAM4 sensitivity curve is shown in Fig. 2(e). Under APD bias of V_{BR}–1V, ROSA sensitivity reaches -19.8dBm at BER=2E-4, and the error floor is ~2E-9. As a comparison, a PD ROSA with same packaging form is also measured, which shows -14.2dBm sensitivity at BER=2E-4. This means APD chips have a 5.6dB sensitivity gain at BER=2E-4 compared with PD chips, thus provides more adequate link budget for 50Gbit/s optical access systems.

4. 50GBaud APD Chips

The 50GBaud APD chips have a similar structure with the 25GBaud APD chips, but with an updated layers thickness to meet bandwidth and responsivity requirements. The corresponding DC and RF testing results are shown in Fig. 3(a) and (b). The breakdown voltage is about 20.3V and the dark current at V_{BR}–1V is about 0.66μA at 25ºC. The responsivity of 1310nm is 6.1A/W at V_{BR}–1V and 3.1A/W at V_{BR}–2V, with primary responsivity estimated to be ~0.45A/W. The bandwidth of the APD chip at V_{BR}–2V is 25 GHz. It should be noted that the bandwidth characteristic of the chip is special optimized, as most 50GBaud TIA usually has a pre-designed S21 curve peaking effect at high frequency band. The pre-designed peaking could enhance the over-all bandwidth, but it might also induce ROSA bandwidth curve show a large peaking in high frequency range if the chip and TIA don't match well. The bandwidth curve of the ROSA is also shown in Fig. 3(b), which shows a flat shape without obvious peaking.

The setup of 50Gbit/s NRZ sensitivity testing is shown in Fig. 3(c). A tunable laser with a $LiNbO_3$ modulator is used as the light source, the modulator is driven by a commercial BERT's PPG module, and a driver is added between the modulator and the BERT to provide a suitable peak-to-peak voltage amplitude. The outer ER of the light source is 8.1dB. Sensitivity is measured by BERT Rx side with a build-in equalizer, as shown in Fig. 3(d). APD ROSA shows -23.2dBm sensitivity at BER=1E-3 with the bias voltage equals V_{BR}–1V, while PD ROSA has a

-17.5dBm sensitivity under same testing condition. The 5.7dB sensitivity gain of APD ROSA brings huge opportunities to 50G PON applications.

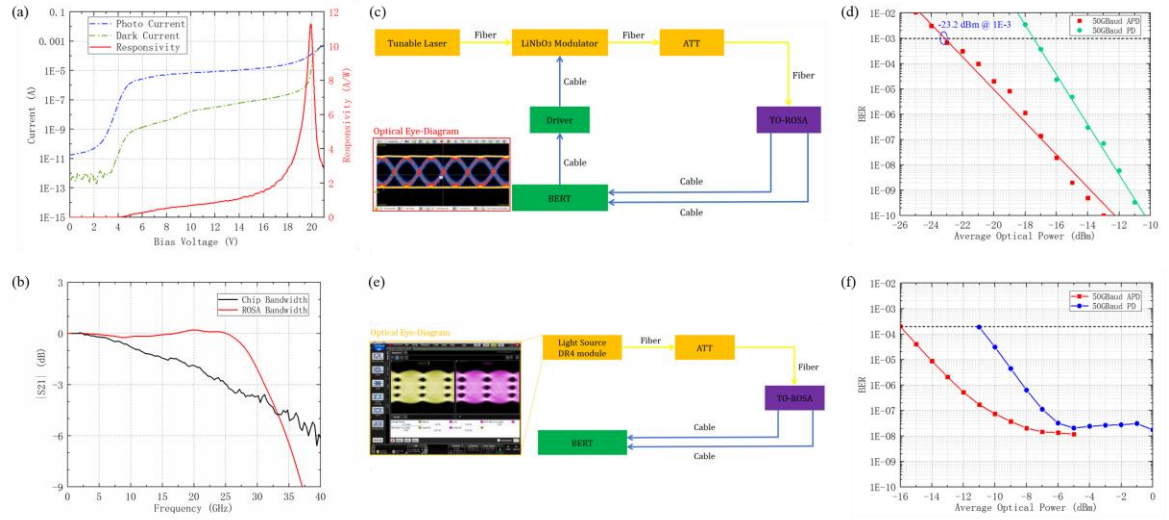
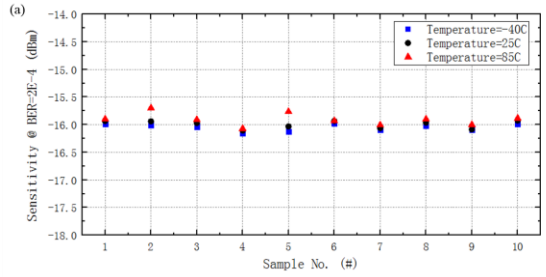


Fig. 3. (a) Photo current, dark current and responsivity curves of 50GBaud APD Chip at 25ºC. (b) RF response of the APD chip and ROSA. (c)-(d) 50Gbit/s NRZ testing setup and BER measurement results of 50GBaud APD ROSA and PD ROSA. (e)-(f) 100Gbit/s PAM4 testing setup and BER measurement results of 50GBaud APD ROSA and PD ROSA.

Similarly, the sensitivity testing and consistency verification of 100Gbit/s PAM4 are also performed. As shown in Fig. 3(e), a 4x100G commercial DR4 transceiver (λ=1310 nm, PAM4) is used as the light source in the testing, with TDECQ=1.4dB and outer ER=5.4dB. The back-to-back 100Gbit/s PAM4 sensitivity curves are shown in Fig. 3(f). The sensitivity is about -16.0dBm at BER=2E-4, and the error floor is ~1E-8, under the bias of V_{BR}–1.5V. As a comparison, a PD ROSA with same packaging form shows -11.0dBm sensitivity at BER=2E-4. APD ROSA also shows about a 5.0dB sensitivity gain compared with PD ROSA, which could extremely expand the application of 50GBaud APD in 100Gbit/s optical access systems, such as 100G ER1 modules mentioned above.

The 50GBaud APD chips also show great consistency, and the 100Gbit/s PAM4 testing results are shown in Fig. 4(a). Sensitivity at temperature range from -40ºC ~85ºC are all around -16 dBm at BER=2E-4, and the error floor are around E-8 level. As shown in Fig. 4(b), the performance of 50GBaud APD can meet 100G-ER1 standard well, and this will greatly help the deployment of 100G ER1 transceiver.



(b)

	100G-ER1-40km standard	50GBaud APD testing results	Unit
PAM4 signal rate	53.125±100ppm	53.125	GBd
Wavelength	1308.09~1310.19	1310	nm
Damage threshold (min)	-2.4	>4.0 (with a 3kohm protection resistor)	dBm
Sensitivity at BER=2.40E-4 (OMA), (max)	-13.8	-15.5~-15.0	dBm
Overload	-3.4	>-2	dBm

Fig. 4. (a) Sensitivity at BER=2E-4 under temperature -40ºC/25ºC/85ºC, respectively. (b) Comparison between 50GBaud APD testing results and 100G-ER1-40km standard.

5. Conclusion

25GBaud and 50GBaud Ge/Si APD chips have been summarized in this paper, and specifications show these devices can be good candidates to be applied in 25GB and 50GB applications like ER and PON scenario. At the same time, advanced CMOS manufacture platform can guarantee high throughput, better device uniformity, and high yield to realize large scale deployment in access optical fiber systems.

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