Low-Loss Wafer-Bonded Silicon Photonic MEMS Switches

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Abstract: We report on 32x32 silicon photonic switches realized through wafer bonding. Broadband operation is demonstrated over 1260-1320 nm range. The maximum on-chip loss is measured to be 4 dB and the cross-talk is -80 dB. © 2022 The Author(s)

1. Introduction

With the ever-increasing demands for high data rates and continual scaling in data centers and for AI and machine learning applications, photonic switches have attracted a great amount of attention due to their energy efficiency and scalability of interconnect networks. Silicon photonic is a promising platform for large-scale photonic switches thanks to its low-cost and mature manufacturing technology available through advanced electronic integrated circuits foundries. While several silicon photonic switches have been demonstrated based on Mach-Zehnder interferometer architecture, their cumulative optical loss of long cascaded chains and large footprint impede the scalability beyond 32 ports [1].

Our group has previously demonstrated novel, highly-scalable, and fast optical switching design based on microelectromechanical-system (MEMS) actuators with nearly zero loss in the BAR (non-switching) state and low loss in the CROSS (switching) state as a promising pathway towards large-scale crossbar switch construction [2]. We have recently reported on a 240x240 switch array with the maximum on-chip loss of 9.8 dB [3]. This has been the largest integrated photonic switch array reported to the date. Although in-plane multi-mode (MMI) crossings with losses as low as 0.016 dB were utilized in this single-layer architecture, scaling the switch network array up to 1000x1000 and beyond would still result in significant optical loss, i.e., ~32 dB, from the crossings alone. This indicates the waveguide crossings to be the main contributing source of optical loss for ultra-large-scale switch networks. Limited bandwidth and poor fabrication tolerance can also be noted for the MMI crossings.

In this paper, we report on a promising pathway towards ultra-large-scale photonic switch arrays by eliminating the in-plane waveguide crossings in the previous work. The novel design is based on a double-layer silicon-on-insulator (SOI) architecture. A robust and void-free wafer-bonding platform has been developed and as a proof of concept, a 32x32 switch array has been demonstrated with the measured maximum on-chip loss of 4 dB, switching time of 1.5, and 0.9 us, for ON and OFF switching times, respectively, cross-talk of -80 dB, and a broadband operation 1260-1320 nm wavelength range.

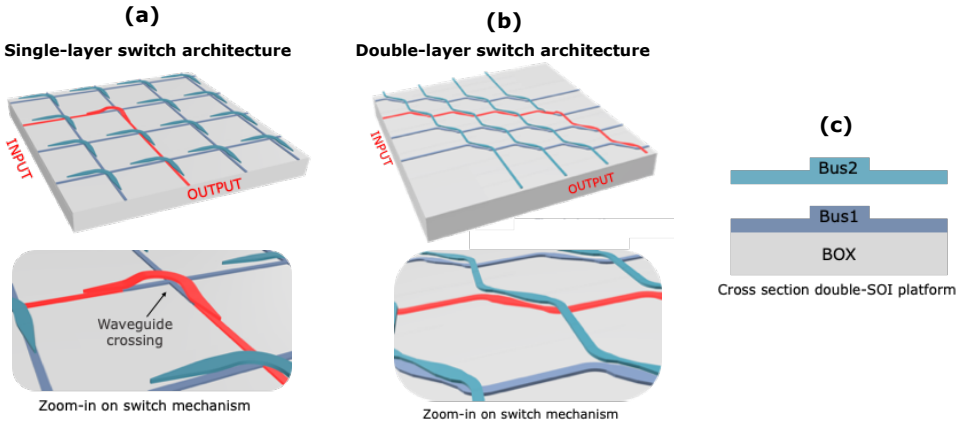

Figure 1. (a) Single-layer architecture consisting of in-plane MMI waveguide crossings. Both input and output waveguides are fabricated are on the same layer. (b) The new double-layer architecture. Input and output waveguide layers are separated. Bus-2 waveguide include the adiabatic couplers. The highlighted red line in (a) and (b) shows an example light path from one input to an output waveguide. (c) cross section of the switch mechanism after MEMS release (showing only the optical coupling element).

2. Switch Architecture and Design

Figure 1(a) depicts the single-layer switch architecture previously demonstrated. As shown in Fig. 1(b), the in-plane waveguide crossings are eliminated with separate input and output layers. Adiabatic couplers are designed to switch light from the bottom-layer input waveguides (Bus 1) to the top-layer output waveguides (Bus 2). Both Bus 1 and Bus 2 layers are rib waveguides with 110 nm partially etch on a 220-nm SOI wafer. The cross section of the optical switching part is shown in Fig. 1(c). A 32x32 switch array is designed in a 1x1.5 cm^2 switch die. 150-nm gap is designed as the switching spacing between Bus1 and Bus2 waveguides, shown in Fig. 1(c). FDTD simulation suggests 0.1 dB coupling loss beyond O band over C band wavelength range.

3. Fabrication and Experimental Result

The fabrication process of the switch starts on the bottom 6-inch 220-nm SOI wafer, as shown in Fig. 2. Grating couplers are formed for input/output coupling. 800-nm wide and 110-nm partially etched ridge Si waveguides are used as Bus 1 and Bus 2. Active topography reduction is performed by etching the deposited LTO to minimize the topography before wafer bonding. Next, a chemical-mechanical polishing (CMP) step is required to ensure the smoothness of the top surface before bonding. To remove any gas by-products from organic residues or trapped air in the bonding interface layer, an array of vertical outgassing channels (VOCs) [4], 7x7 um^2, are etched into the top 6-inch SOI wafer before the bonding step. Then, the top substrate and BOX layers are removed. It should be noted that both active topography reduction and VOCs are necessary to achieve a void-free and smooth transferred c-Si layer as Bus 2 waveguides and couplers. The result of a successful wafer bonding showing zero interfacial void is shown in Fig. 3(a). Finally, the top Si waveguides are patterned, the MEMS actuator is fabricated, and the devices are released in vapor HF. The MEMS actuator fabrication is not discussed here for simplicity. A scanning electron microscope (SEM) image of the fabricated switch can be found in Fig. 3(b).

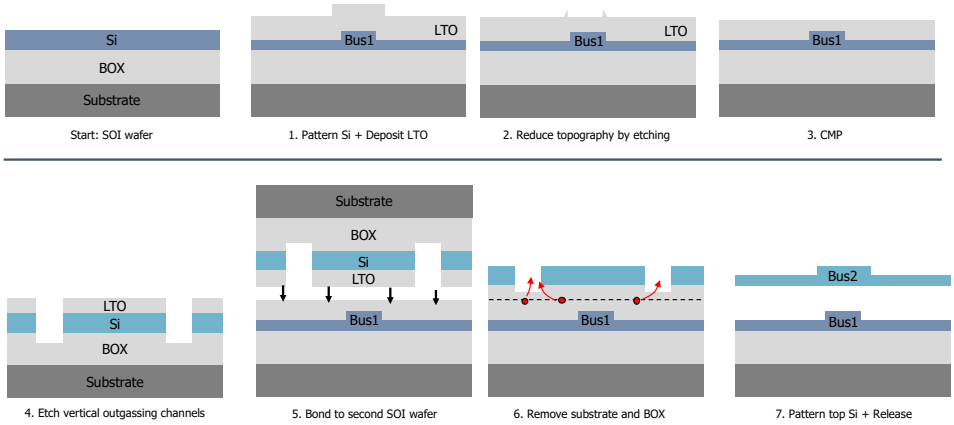

Figure 2. Overview of the fabrication steps. The MEMS actuator fabrication is not included in the figure for simplicity. Steps 2-4 are necessary in order to achieve a void-free transferred c-Si layer. Steps 6 shows the absorption of any generated gas byproduct which moves to the nearest outgassing channel and gets absorbed through the BOX layer.

The 32x32 switch array is experimentally characterized using two 72-channel fiber arrays for optical input and output by coupling via grating couplers with a coupling loss of 4 dB/facet. Electrical probes are used to actuate the switch cell and the results are shown in Figs. 3(c) and 3(d). The ON and OFF switching times are measured to be 1.5 and 0.9 us, respectively. The switch exhibits a high ON/OFF extinction ratio of ~80 dB. Over 100 switch configurations are measured to characterize the on-chip loss of the switch array. As depicted in Fig. 3(e), 0.47 dB/cell is extracted from linear fitting and the longest on-chip loss is measured to be 4 dB. The Bus1 and Bus2 waveguides loss are measured to be 1.3 and 1.9 dB/cm, respectively, from test structures. The higher amount of loss for Bus2 waveguides can be attributed to the cleanliness of the waveguide or the bonded interface pressure, since the waveguide test structures were measured before release. Broadband operation of the switch is depicted in Fig. 3(f) over the 1260-1320 nm wavelength range.

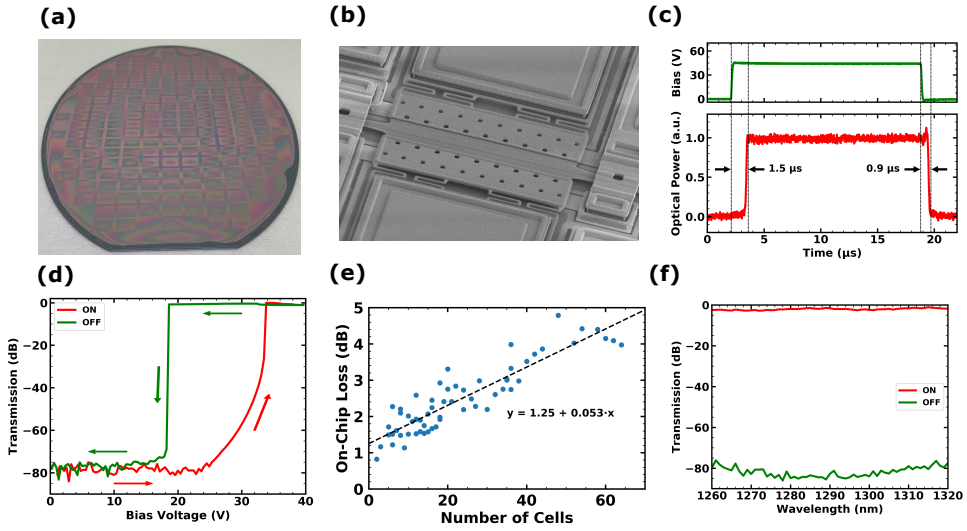

Figure 3. (a) Void-free wafer bonding result. (b) SEM micrograph of a single switch cell. (c) Measured actuation voltage of the poly-Si switch along with the ON and OFF switching times. (d) Measured switch transfer curve. (e) On-chip loss measurement with various switching cells. (f) Measured transmission curve of the switch for various wavelengths.

In summary, we have demonstrated a 32x32 silicon photonic switch network on a double-layer SOI architecture through wafer bonding. Active topography reduction and vertical outgassing channels are utilized to achieve void-free wafer-bonded platform. The measured switching loss for one input switch and one output switch is 1.12 dB. The maximum on-chip loss is measured to be 4 dB and the crosstalk is below -80 dB. The switch exhibits broadband operation. The ON and OFF switching voltages are 33 and 17, while the switching times are 1.5, and 0.9 us, respectively.

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4. References

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