Optical Content Addressable Memory Matchline and RAM table Encoding/Decoding using an integrated CAM cell

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Abstract: We experimentally demonstrate for the first time an all-optical fully-integrated InP CAM cell within a complete CAM Matchline architecture with RAM table Encoding and Decoding functionalities. Error-free operation has been evaluated at 5 Gb/s.
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1. Introduction

With the frantic scaling of linerates beyond 400 Gb/s along with the rise of Big Data or Low-Latency applications, the increasing demand for high-bandwidth and low-latency optical-interconnectivity have been pushing for faster information processing engines and higher-rate routing operations [1]. In parallel, owing to the continuously growing number of connected devices, the Routing Information Tables (RIT) have been following a similar trend towards larger table entries. This reveals a constantly increasing need for faster header processing time for Address Lookup (AL) operations, leading to a significant performance and latency bottlenecks in network-operations [2]. Although, electronic Content Addressable Memories (CAMs) are designed to handle intensive applications, enabling fast AL operation across the whole CAM-table in a single clock cycle [3], their speed still rarely exceeds the 1GHz regime[4].

To this end, optical memory technologies can support higher datarates, achieving recently to release a series of high-speed photonic RAMs [5], CAM cells [6] and integrated memories [7][8], which can be utilized for fast router AL functionalities. First experimental demonstrations of high-speed optical CAM cells have shown 10 times higher speeds than their electronic counterparts [9], allowing for building fully functional Matchline (ML) [6] architectures and Ternary-CAM (T-CAM) configurations, that can look-up directly in the optical domain a 2-bit destination address [10]. Yet, the transition from CAM Matchline layouts to complete optical router look-up table configurations requires an integrated CAM cell technology as well as an all-optical RAM table Encoding and Decoding circuit for interpreting the matched CAM line output and triggering the correct RAM table entry for subsequent forwarding operation [11].

In this work, we present for the first time to our knowledge, an optical CAM ML architecture employing a fully integrated photonic CAM cell and a novel all-optical RAM table Encoding and Decoding circuit architecture. The proposed configuration exploits a 2-bit optical CAM line and successfully designates whether the incoming optical address matches the optical address stored in the CAM line, forwarding the ML output signal to the correct RAM row entry via a wavelength conversion and routing scheme utilized for Encoding/Decoding operations. The CAM line employs an all-optical fully-integrated binary CAM cell, which relies on a generic monolithically integrated InP SOA-based Flip-Flop (FF) memory and a Semiconductor Optical Amplifier (SOA) – Mach Zehnder Interferometer (MZI) XOR Access Gate (AG) co-integrated on the same chip. Encoding and Decoding is carried out via an additional discrete SOA-MZI-based wavelength converter followed by an Arrayed Waveguide Grating Router (AWGR). Proof-of-principle operation has been experimentally evaluated at 5 Gb/s for all possible CAM line contents and Encoding/Decoding combinations, revealing error-free operation with a total power penalty of 7.9 dB.

2. Device and Experimental Setup

Fig.1 (a) shows the conceptual schematic of a complete AL table when 2-bit long addresses are used both in the CAM and RAM tables. The incoming address, denoted as search word, is simultaneously compared with all CAM

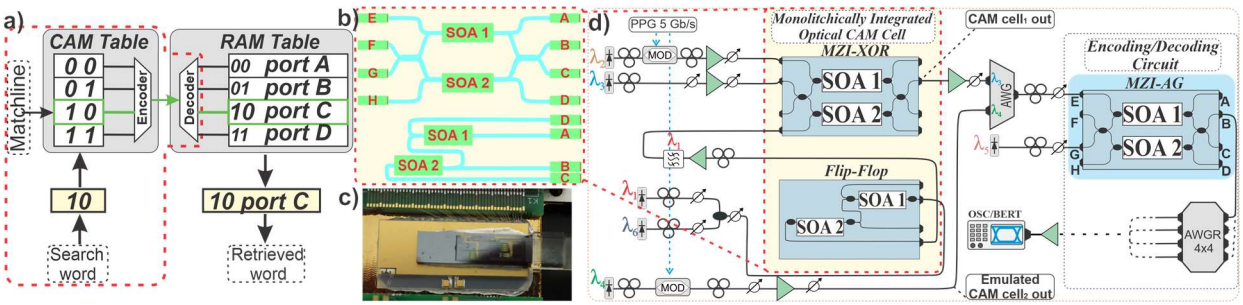

Fig.1. a) Schematic of AL table, b) chip layout of FF memory and SOA-MZI AG, c) Photo of the electro-optic packaged chip, d) Experimental setup of the 2-bit match-line, encoding and decoding operation.

table entries, producing a *"match"* signal only at the CAM row that includes an identical word. This *"match"* signal has to be directed to the correct RAM table entry via an Encoding/Decoding circuit for allowing access to this specific RAM row. The RAM row that stores the correct router output port address that corresponds to the desired destination will be activated to emerge at the AL output. The red-highlight area including the CAM table and Encoding/Decoding circuitry depicts the configuration under study. Fig.1 (b) presents the mask layout of the monolithically integrated InP chip that was used as one of the two CAM cells within the 2-bit CAM line, fabricated at a MPW run of Fraunhofer HHI, including two cross-coupled SOA-XGM switches as an optical flip-flop together with a SOA-MZI gate that offers the XOR functionality. A photo of the packaged PIC is shown in Fig.1 (c).

Fig.1 (d) shows the experimental setup of the proposed CAM-ML architecture. One of the two CAM cells was based on the integrated CAM cell, while the second CAM cell output was emulated by an optical data generation module. Encoding/Decoding operation was provided by an additional discrete SOA-MZI Access Gate (AG) that performs as a wavelength converter and is followed by a 4-port AWGR. Two CWs signals at λ_2=1550 nm and λ_4=1551.2 nm by tunable laser sources (TLS) were modulated by Ti:LiNbO3 modulators at 5 Gb/s Programmable Pattern Generator (PPG) with NRZ 2^7-1 PRBS-based data-streams. The data-signal λ_2 acts as a search bit in the integrated optical XOR gate via port E, along with the CW λ_3 at 1535.2 nm via port F, as input signals of the SOA-MZI XOR gate. Furthermore, two CWs (λ_1, λ_6) at 1547.2 nm and 1548.2 were fed as pump light via port A in the integrated optical Flip-Flop (FF), which was configured to operate at one of the two optical FF states, with detailed description of the Write operation to define the state of the bistable photonic memory found in [12]. The optical output of the bistable FF memory was collected through port C and was filtered by an optical bandpass filter, and inserted through port H, into the integrated SOA–MZI XOR gate, in order to feed the stored bit-signals to the XOR-based comparison.

The optical CAM output and logical content of the XOR between λ_1 and λ_2 was imprinted at λ_3 signal. Moreover, the modulated signal that was imprinted on λ_4 emulates the search output result of the second CAM cell. The optical signals at λ_3 and λ_4 were multiplexed with the use of an AWG multiplexer, producing in this way a multi-level ML signal at the output of the AWG, that is passed to the Encoding/Decoding Circuit through port E. A CW signal at λ_5 was produced by a TLS and was fed into the MZI-AG via port G to form its input signal. In this way, the multi-level signal gets transformed into a binary NRZ waveform and wavelength-converted onto λ_5, with the MZI-AG output beam collected at port B and being forwarded to a 4-port AWGR. Depending on the exact λ_5 wavelength value, the λ_5-wavelength-converted match signal will be wavelength-routed by the AWGR to a certain output port and directed to the appropriate RAM row. As such, the CAM/RAM row mapping adopted in the router AL is defined by the exact λ_5 wavelength value enforced at the MZI-AG input. EDFAs, VOAs and PCs were used to tune the signals at 19.5 dBm for λ_2 and λ_3 signals, 14.5 dBm and 20 dBm for λ_1 and λ_5 respectively and the power of the multi-level signal at 3 dBm. The FF SOAs were driven at 200mA, and around 160 mA and 280 for the MZI-XOR and MZI-AG, respectively.

3. Experimental Results

Fig.2 (a)-(d) show the synchronized time traces and eye diagrams of the principle of the 5Gb/s InP CAM cell. Fig.2 (a) shows the stored bit of the optical FF at λ_1, of the CAM cell corresponding to the logical '0' or logical '1' state. The FF memory has also been evaluated for Write operation, at 5 Gb/s [12]. Fig.2 (b) depicts the time traces of the Search-Line (SL) signal, prior being injected in the optical CAM cell. The resulting traces of the CAM cell output are shown in Fig.2 (c) and Fig.2 (d) depicts their respective eye diagrams. The eye diagrams of the respective single-bit

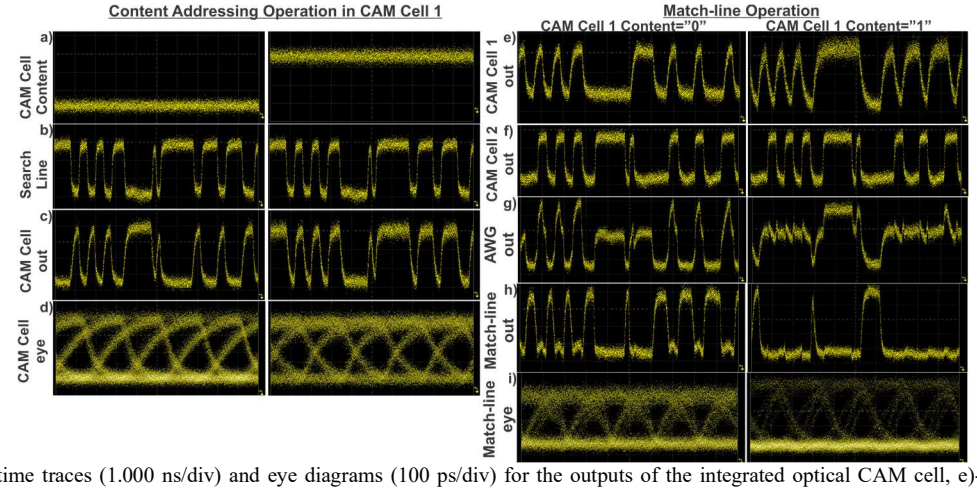

Fig.2. a)-d) time traces (1.000 ns/div) and eye diagrams (100 ps/div) for the outputs of the integrated optical CAM cell, e)-i) Match-line operation time traces (1.000 ns/div) and eye diagrams (100 ps/div), for CAM cell 1 Content = "0" and CAM cell 1 Content = "1".

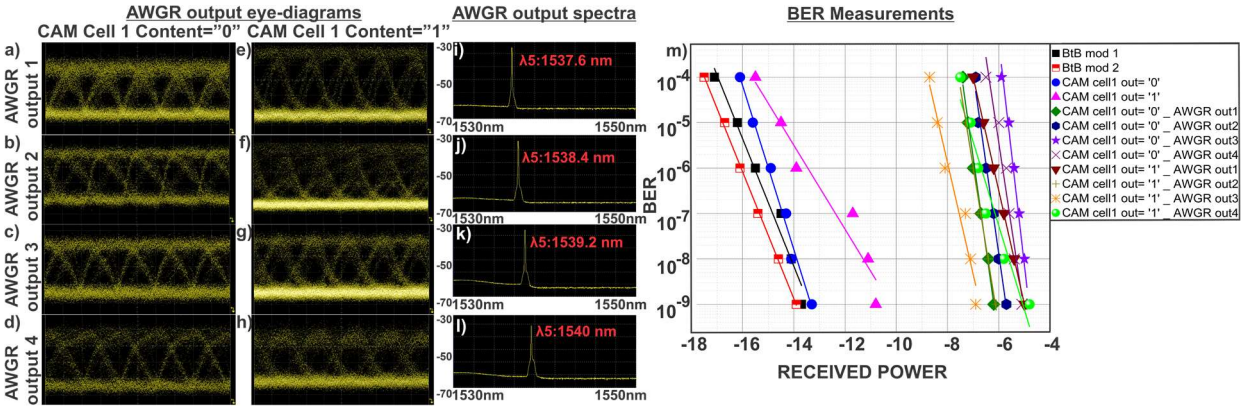

Fig.3. a)-d) eye diagrams (100 ps/div), for CAM cell 1 Content = "0", e)-h) eye diagrams (100 ps/div), for CAM cell 1 Content = "1", i)-l) AWRG output spectra and m) BER curves for BtB, XOR operation and ML operation, at 5Gb/s.

search operation of the CAM cell, exhibit clear eye openings with an Extinction Ratio (ER) of 5.8 and 7.7 dB, respectively. Fig.2 (e)-(i) present the 2-bit operation of the ML. Fig.2 (e) and (f) show again the output traces of the CAM cell$_1$ and CAM cell$_2$, respectively, in a different time window. The combination of these two signals with the use of the AWG multiplexer produces the multi-level signals, illustrated in Fig.2 (g), exhibiting three different power levels, corresponding in every case to a different number of bit-level search miss. The result of ML trace at the output of the MZI-AG is depicted in Fig.2 (h). As shown in Fig.2 (h) a logical '1' appear only in the case of a match between both the search bit and stored bit, while in every other case the result is a logical '0'. The respective eye diagrams of the ML operation are being illustrated in Fig.2 (i), revealing an ER of 6 and 6.8 dB, respectively.

The performance of the complete ML and decoding architecture was evaluated through eye diagrams and BER measurements, as shown in Fig.3. Fig.3 (a)-(d) present the eye diagrams of every output port of the AWGR, in case the CAM cell$_1$ content is a logical "0" and (e)-(h) the case, where the CAM cell$_1$ content is a logical "1", with an ER of around 6 dB and 6.5 dB, respectively. Based on the functionality of the AWGR, every discrete wavelength of λ_5, which is inserted in one of the ports of the AWGR, is forwarded to every one of its four outputs ports. For all the four cases of λ_5, the specific scheme, of the MZI-AG and the AWGR, implements a complete 4x4 Encoding-Decoding process. Fig.3 (i)-(l) show four indicative spectra of every wavelength of λ_5 [1537.6-1540] nm at the four outputs of the AWGR. Finally, the BER curves of the Back-to-Back (BtB), XOR operation and AWGR outputs, are illustrated in Fig.3 (m). Error-free operation was achieved for all the experimental stages of the integrated CAM cell along with the ML and decoding operation. Compared to the BtB signals, the XOR operation for a logical "0" of the CAM cell$_1$, features a BER penalty of 0.5 dB, and a penalty of 2.8 dB for the case of logical "1". The AWGR outputs indicate a total power penalty of around 7.9 dB, for both cases.

4.Conclusions

The first all-optical 2-bit CAM Matchline with Encoding/Decoding operation is experimentally demonstrated at 5Gb/s error free operation, towards building a complete, ultra-fast Address Look-Up operation at fast, low-latency routers.

Acknowledgements

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5. References

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