16-bit (4x4) Optical Random Access Memory (RAM) Bank

Christos Pappas, Theodoros Moschos, Theoni Alexoudi, Christos Vagionas and Nikos Pleros
Centre for Interdisciplinary Research and Innovation, Informatics Dept. Aristotle University of Thessaloniki, Greece
Author e-mail address: chripapp@csd.auth.gr

Abstract: A complete 16-bit all-optical RAM bank capable of storing 4×4-bit WDM-formatted optical data words at a 20Gb/s memory-throughput is experimentally presented for the first time, using sixteen 5Gb/s monolithic InP Flip-Flops and all-passive Row/Column Decoding circuits.
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1. Introduction

Over the past years, the increase in processor throughput is exceeding the electronic memory speed progress revealing a gap between the CPU-Memory performance and limiting the system's performance to slower operating frequencies of the electronic memories, problem also known as "Memory Wall" [1]. To this end, Optical Static Random-Access Memories (SRAMs) seem to form a competitive alternative to electronic Static RAMs for increasing read/write access speeds, reducing memory access times, footprint and power requirements, and allowing for multi-bit optical memory operation [2]-[7]. So far, most optical memory demonstrations have been limited to elementary latching units without even encompassing an optical Access Gates (AGs) for ensuring the control of Random-Access functionality, as is traditionally offered by electronic SRAM for controlling the communication of the memory cell with the "outer world". Only a few architectures have so far demonstrated true random-access functionality advancing up to 10Gb/s for a single-bit RAM memory unit [3] and up to 20Gb/s memory throughput for a 4-bit WDM-enabled optical RAM Row [4], with the latter confirming the efficient scaling towards multi-cell optical RAM layouts. Migrating, however, to practical multi-bit all-optical RAM implementations requires the evolution from simple memory elements and RAM rows into fast and fully functional optical multi-bit addressable RAM banks, where cooperation with system-level optically enabled peripheral circuitry is necessary [9]. This has been demonstrated so far only via physical layer simulations within a complete design of an optical cache memory [9], with experimental RAM demonstrations never going beyond single Row developments.

In this paper, we report on the first experimental demonstration of a WDM-enabled 16-bit Addressable Optical RAM Bank organized in a 4×4 layout with 20Gb/s random-access at every of the four Word Lines (WLs). The Optical RAM Bank is addressed via a passive filter-based Optical Row Decoder (RD) circuit and a passive demux-based Column Decoder (CDs). Our novel concept minimizes the active AG devices by exploiting a single multi-λ AG device per WL, while enabling complete all-passive Row/Column decoding through λ-demux devices. The proposed architecture includes a 4×4 WDM-enabled RAM bank comprising four optical RAM Rows [4], with each row incorporating four discrete fully packaged monolithic integrated Indium Phosphide (InP) optical Flip Flops (FFs) connected via an AWG-based CD circuit to a single multi-λ SOA-MZI AG. A filtering bank formed by four Arrayed Waveguide Grating (AWG) pairs comprises the RD circuit. Experimental verification is achieved at 4×4×5Gb/s with 8.3-10.2 dB peak power penalty for all 16 InP RAM cells.

2. Device and Experimental setup

The experimental setup employed for the evaluation of the 16-bit RAM Bank with 20Gb/s throughput is depicted in Fig. 1 and comprises an all-passive RD circuit for selecting one out of the four available WLs, a hybridly integrated SOA-MZI AG per WL, an AWG-based demultiplexer serving as the passive CD and a 4×4 RAM bank consisted of four cascaded RAM Rows [4]. Every row includes four monolithically integrated discrete InP FFs for a total of 16-bit optical storing. Two AWGs multiplex 12 Continuous-Wave (CW) beams at odd and even λs, to produce two WDM streams. These streams were injected into two different $LiNbO_3$ Mach- Zehnder modulators (MOD), driven by a 5 Gb/s programmable pattern generator (PPG) to generate pairs of complementary 5 Gb/s Non-Return to Zero (NRZ) pseudorandom binary sequence (PRBS) $2^7 - 1$ -based custom patterns, creating the 8-wavelength 4-bit WDM words (λ1-λ8) and the 4-wavelength 2-bit Access Signals (λ9-λ12). Then, a 50/50 coupler was used to combine the two MOD outputs and create two distinct paths, the 4-bit WDM data words and the four AS through the RD. The RD incorporates four AWG pairs so that every pair corresponds to one out of the four possible WLs. For equally optical power distribution the four pairs were connected with couplers of different coupling ratio [9]. To achieve bit-level synchronization between the Access Signals and the 4-bit words, and to decorrelate the four data pairs, optical delay lines (ODLs) were used as shown in the setup. In this way each pair of co-propagating complementary data signals share the same peak power, operating altogether as four "effective" CW signals, mitigating any pattern effect between different pairs. For each WL, a dedicated SOA-MZI AG was responsible for granting access to the line or not, while at each timeslot only one WL is permitted to alternate the

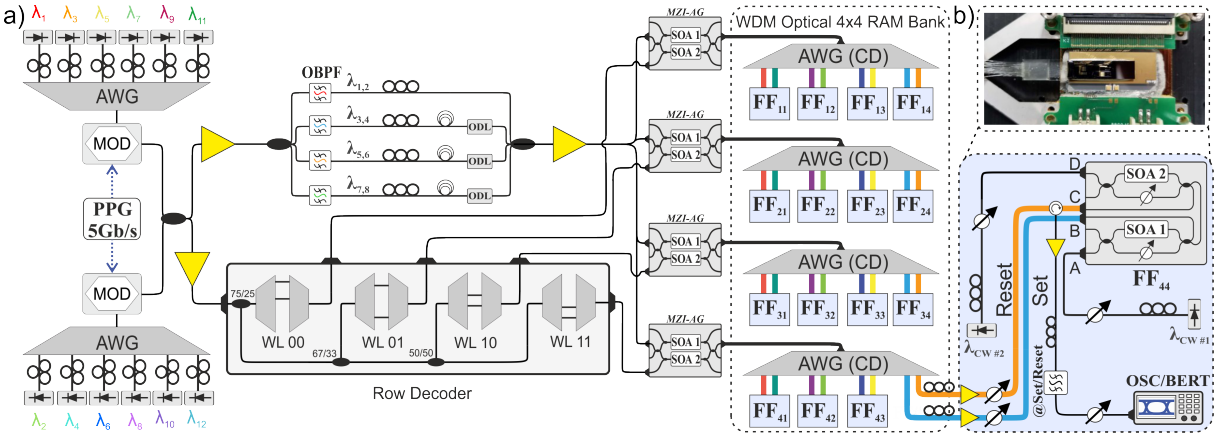

Fig. 1: (a) Experimental setup for the 16-bit RAM evaluation with 20 Gb/s memory throughput and (b) Photo of one out of the sixteen indicatives InP RAM cells.

FFs' contents. Each AG output was connected with an AWG acted as the passive CD circuit to produce the four Set and Reset pairs for every FF in a WL.

The 4×4 RAM bank consisted of 16 discrete FFs, each following the "master-slave" configuration [3], as presented indicatively in the experimental setup for FF_{44} within the light blue inset of Fig 1. Every RAM cell relied on a monolithic InP FF-chip that was fabricated by HHI and fully packaged by PHIX as shown in Fig. 1(b), in terms of optical and electrical contacts for system level testing. Temperature stability was provided by a Peltier cooler along with a thermistor (NTC) attached to the ceramic package and operational temperature was set to 21ºC. A fiber-array was aligned with the I/O of the chip and attached using strain relief. The remaining fifteen FF units follow the same rational, but their detailed configuration was omitted only for simplicity reasons. Both MZIs of the FF were powered by λ_{CW1} and λ_{CW2}, respectively. The FF state signals were led into the 5 Gb/s bit-error rate tester (BERT) and oscilloscope (OSC) for further quality signal evaluation, via two circulators from the same ports that the Set/Reset signals entered the chip. All AGs SOAs were electrically driven by [190-225] mA, while the SOAs of the FFs were driven by [210-250] mA. To maintain proper signal polarization and power levels, polarizer controllers (PCs), variable optical attenuators (VOAs) and erbium-doped fiber amplifiers (EDFAs) were used. Optical Bandpass Filters (OBPF) of 0.6 nm and 1 nm 3dB bandwidth were also utilized for wavelength filtering.

3. Experimental results

The operation of the 16-bit WDM-enabled optical RAM was evaluated for all 4×4×5Gb/s incoming NRZ data streams forming the 4-bit WDM data words and the obtained experimental results of an indicative FF output for each one of the four WLs are illustrated in Fig. 2(a). Each column of Fig. 2(a) refers to the synchronized pulse traces for one FF of each WL (WL "00" - WL "11"), depicting the traces of the incoming word bits (B1-B4) and the four Access Signals (AS1-AS4) in the first two rows and the output of the FF operation (FF_{11}, FF_{22}, FF_{33}, FF_{44}) at the third row. Random access is granted to the respective WL only in case AS has a logical value of "0", in any other case access is blocked. In the second and third columns, the FF outputs are constant "1" and "0" due to absence of Reset and Set pulses, respectively. The respective eye diagrams for the depicted FF output traces are presented in Fig. 2(b), featuring an extinction ratio (ER) of 2.6 dB. Pattern effect mitigation and signal shape improvement is

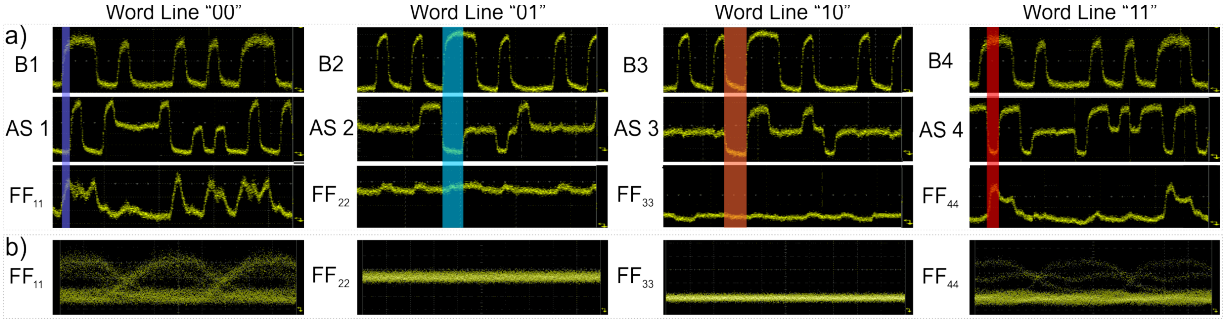

Fig. 2: Experimental results of the 16-bir RAM memory Write operation (a) pulse traces for proof of operation, in every Word Line only one Flip-Flop output is presented for simplicity reasons and (b) the respective eye diagrams. Time scale is at 500ps/div for pulse traces and 50ps/div for eye diagrams.

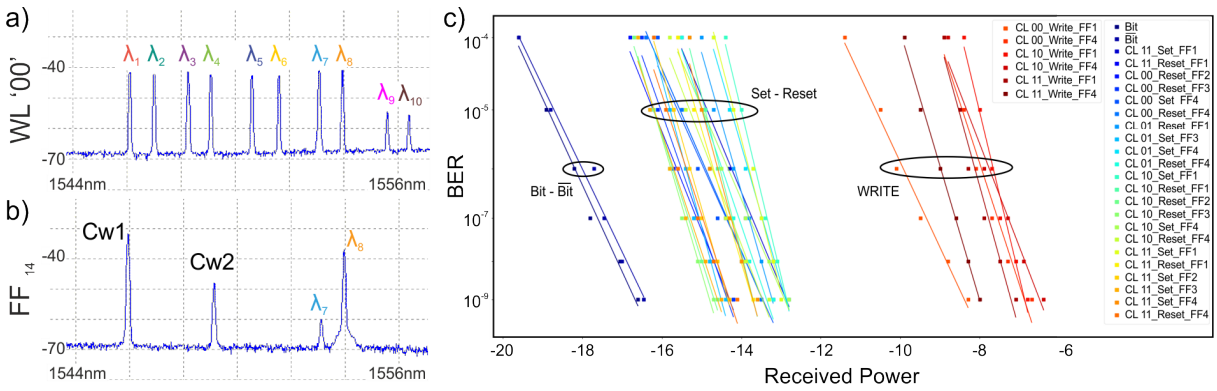

Fig. 3: (a) spectrum obtained after the AG1, for WL"00" where 8×5Gb/s WDM signals were transmitted simultaneously (λ1-λ8) controlled by the Access signals at λ9-λ10, (b) spectrum obtained at FF 4 output and (c) BER curves for Write operation against Set, Reset and bit, $\overline{bit}$ signals serving as Back-to-Back signals.

achieved through SOA-MZI saturation for level "1"and by employing pairs of complementary signals that suppress noise in logical level "0".

Fig. 3(a) shows the optical spectra measured by the optical spectrum analyzer (OSA) at the SOA-MZI-based AG output of WL "00", during Write operation, featuring 8 simultaneously transmitted wavelengths (λ_1-λ_8) of the 4-bit WDM encoded data word along with their respective access signals (λ_9, λ_{10}). The power levels of all transmitted data word signals were equalized at the SOA-MZI output featuring CW-like signals that were fed into the CAS

module to achieve similar memory performance for all optical RAM FF cells. The wavelength and the power levels were aptly selected, in order to minimize undesirable four wave mixing (FWM) phenomena. Fig. 3(b) presents the four wavelengths that were obtained at the output of FF_{14} (WL"00" – FF4) revealing FF operation, with the combination of the two CW signals (CW_1, CW_2) at 1545.6 nm and 1547.5 nm and the control signals Set (λ_7) and Reset (λ_8) at 1553.5 nm and 1555 nm, respectively. Finally, the efficiency of the RAM memory architecture was evaluated for every individual memory cell of the 4×4 RAM bank during Write operation at 5Gb/s, through bit error rate (BER) measurements, as shown in Fig. 3(c). Compared to the Back-to-Back (bit, $\overline{bit}$) signals, the Set and Reset signals feature a total power penalty of 2.5-4 dB and 1.7-3.6 dB, respectively, and the memory cells outputs show total power penalties of 8.3-10.2 dB.

4. Conclusion

A novel optical 16-bit RAM memory architecture with 20Gb/s throughput is experimentally demonstrated, comprising 16 optical FFs for storage in a 4×4 RAM bank configuration, all-passive Row and Column Decoders and multiwavelength shared AGs. The results verify successful random-access of 4-bit WDM-formatted data words between the four WLs, as stipulated by the results, while error-free operation achieved for Write operation with peak power penalties within the range of 8.3-10.2 dB.

Acknowledgements

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