Highly power-efficient (2 pJ/bit), 128Gbps 16QAM signal generation of coherent optical DAC transmitter using 28-nm CMOS driver and all-silicon segmented modulator

Yohei Sobu[1,2], Guoxiu Huang[2], Toshihiko Mori[1,2], Yukito Tsunoda[1,2], Takuji Yamamoto[1,2], Shinsuke Tanaka[1,2], and Takeshi Hoshida[2]

1 Photonics Electronics Technology Research Association (PETRA) 1-20-10 Sekiguchi, Bunkyo-ku, Tokyo, 112-0014, Japan
2 Fujitsu Limited, 4-1-1 Kamikodanaka, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8588, Japan
E-mail: sobu.yohei@fujitsu.com

Abstract: We demonstrated a highly power-efficient coherent optical digital-to-analog converter transmitter. 2pJ/bit operation was realized by combining an all-silicon segmented modulator and a CMOS inverter driver. The bit-error-rate was less than the 25.5% of SD-FEC limit. © 2022 The Author(s)

OCIS codes: (250.4110) Modulators, (230.3120) Integrated optics devices

1. Introduction

Future communication systems require both larger transmission density and higher energy-efficiency than existing systems for optical transceivers. Silicon photonics technology is a promising platform that provides significant advantages in terms of its size, cost, and power consumption compared to conventional technologies. Although silicon photonics has already been developed as a commercial technology, further improvements are under investigation [1]. Recently, the Optical Internetworking Forum launched an 800G coherent project. The transmission capacity must be doubled while almost the maintaining form factors and the transmission distance; particularly, it is necessary to double the energy efficiency. From this viewpoint, improving the energy efficiency of the optical transmitter, such as an optical modulator driver and an electrical digital-to-analog converter (DAC), would be crucial in the future.

The use of an optical DAC architecture is one of the promising solutions for achieving a low-power consumption optical transmitter [2]. This architecture does not require an electrical DAC and a power-hungry large-swing linear driver. The optical DAC transmitter synthesizes digital signals in the optical domain using a segmented modulator and binary-driven driver array. In this architecture, extremely low-power operation can be realized using a complementary metal oxide semiconductor (CMOS) inverter driver with lower amplitude. The concept of optical DACs has been demonstrated using four-level pulse amplitude modulation (PAM) modulation schemes and 112.5 Gbps 16 quadrature amplitude modulation (QAM) with a low power-efficiency of ~4 pJ/bit [3, 4].

Thus far, we have developed an extremely low-power operation (1.59 pJ/bit) of a 56 Gbps PAM4 optical DAC transmitter [5]. This result was characterized by a highly efficient forward-biased positive intrinsic negative (PIN) phase shifter integrated with a resistance and capacitance equalizer (PIN-RC). Subsequently, we demonstrated the feasibility of high-speed PIN-RC modulator at 90 Gbaud NRZ and 70 Gbaud PAM4 with a wide EO 3-dB bandwidth of 43.9 GHz [6]. In this study, we applied the optical DAC architecture to a coherent optical transmitter to realize a promising next-generation transceiver. A highly power-efficient (2 pJ/bit) coherent optical DAC transmitter of 128 Gbps 16QAM operation was successfully demonstrated.

2. Optical DAC transmitter design and fabricated device

Figure 1 (a) shows a fabricated optical DAC transmitter. A single polarization IQ segmented modulator was integrated with a CMOS inverter driver via flip-chip bonding. The photonics integrated circuit (PIC) has RF and DC metal probing pads and optical coupling ports. The footprint of the CMOS driver chip is as small as 1.0×3.0 μm^2. For 16QAM operation, the IQ modulator has three segments, each of whose length is 250 μm, as shown in Fig. 1 (b). In this case, the left segment corresponds to the least significant bit (LSB) and the other two segments correspond to the most significant bit (MSB). The driver chip includes all the circuit blocks shown in Fig. 1 (c). The driver comprises CML input buffers of 100 Ω termination, level shifters, and CMOS inverter drivers (F.O. = 2). The MSB signal was divided into two segments after level shifters. The multi-stage inverter drivers of the MSB and the LSB were arranged in the vicinity of the output bumps connected to the PIC. The CMOS driver chip was fabricated using TSMC 28-nm CMOS technology. Figure 1 (d) shows the schematic cross-sectional view of the PIN-RC phase

shifter fabricated using a general silicon photonics foundry according to only their baseline process. The passive RC equalizer expands the limited modulation bandwidth of the PIN phase shifter. The phase shifter performance can be easily optimized using this structure, considering the trade-off between the modulation bandwidth and efficiency [5, 6]. This RC equalizer was composed only a simple passive component.

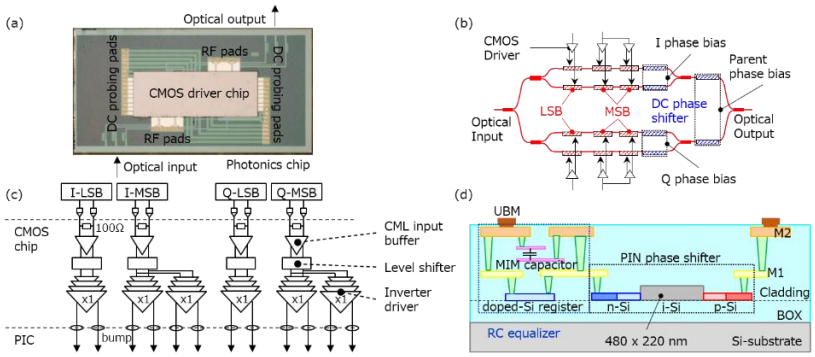

Fig. 1. (a) Top view photograph of the integrated optical DAC transmitter. (b) Structure of the three segmented IQ-MZM for 16QAM operation. (c) Schematic block diagram of the driver chip. (d) Schematic cross-sectional structure of the PIN-RC modulator.

3. Experimental setup and performance of the optical DAC transmitter

The experimental setup of a 16QAM optical DAC transmitter used to measure the bit-error-rate (BER) performance is shown in Fig. 2. We used an arbitrary waveform generator (AWG, Keysight, M8196A), RF phase matching cables, and RF probes (Form Factor, Infinity Quad Probe) to input the differential drive signals into the metal probing pads on the PIC. The frequency responses of the AWG and RF cables were compensated by the AWG. The modulated optical signal was amplified using an EDFA. Then, coherent detection was performed using a high-bandwidth integrated coherent receiver (HB-ICR, Fujitsu) and recorded using a digital storage oscilloscope (DSO-X, Keysight, 93204A, 80GSa/s). ASE (amplified spontaneous emission) noise was added to the output modulated signal to measure the OSNR performance. The signal quality of the coherent optical DAC transmitter was evaluated using an offline DSP. The constant modulus algorithm and Viterbi and Viterbi phase recovery algorithm were employed for the adaptive equalizer (AEQ) and carrier phase recovery (CPR) blocks. The minimum means square error filter was used after the CPR to compensate for the Tx imperfection. Finally, the BER was measured. The baud rate was varied from 25 to 32 Gbaud for 16QAM operation. The input data to each segment are 282624 samples extracted from PRBS20. The operating wavelength was 1552.524 nm.

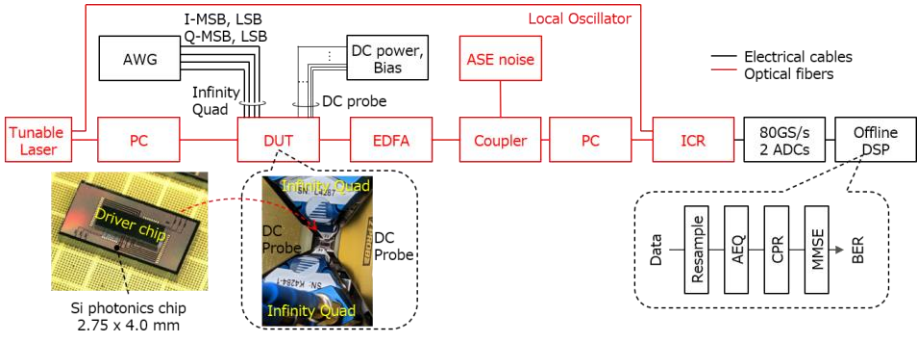

Fig. 2. Single polarization 16QAM experimental setup with a PIN-RC based IQ modulator

First, the integrated transmitter was evaluated in NRZ and PAM4 operation to confirm its basic modulation characteristics. We measured an optical output waveform and an extinction ratio of each child-MZI. In NRZ operation, only LSB or MSB data was fed into the transmitter. The output optical waveforms and the extinction ratio at 32 Gbaud are shown in Fig.3 (a). The bias current of the PIN-RC phase shifter was adjusted to 0.9 mA at a single arm of the child-MZI to inject a sufficient electric charge into the PIN diode. The $V\pi L$ of PIN-RC phase shifter was measured as ~0.4 Vcm at this bias current. The transmitter exhibited clear eye-openings with NRZ and PAM4 operation, and the extinction ratio corresponded to the design value. The waveform quality in LSB of the I-MZM was slightly degraded by manufacturing yield. Although this degraded waveform quality causes the limitation of the transmitter performance, it is not an essential issue in this architecture.

Then, we investigated 16QAM operation of the transmitter. All circuits, including the LSB and the MSB of the IQ modulator, were operated. The bias points of the child- and parent-MZI were adjusted to the null- and quadrature-point, respectively. The optical propagation loss of the phase shifter was measured to be 20 dB/cm, which corresponds to a modulator insertion loss of 1.5 dB. The modulation depth of 16QAM operation was estimated to be ~±0.3π. Four random uncorrelated data were entered into the I-LSB, I-MSB, Q-LSB, and Q-MSB segments, and then the timing skews were adjusted manually using the AWG. The input signals were multiplexed to generate the 16QAM constellation in the optical domain. Figure 3 (b) shows the BER vs. the OSNR performance. At 32 Gbaud, the measured BER was less than the SD-FEC limit and saturated around 1.0×10^{-2}. By stepping down the baud rate to 28 and 25 Gbaud, better results were obtained. The BERs were less than the HD-FEC limit and improved to 2.0×10^{-4}. Figure 3 (c) shows the 16QAM constellation of the optical signal and the power-efficiency performance. The power consumptions of a CMOS inverter driver combined with a biased current for a PIN phase shifter were measured to be 219, 238, and 261 mW at a baud rate of 25, 28, and 32 Gbaud, respectively. These measurements correspond to high energy efficiencies of ~2 pJ/bit, which is 50% less than the results of previous studies on a coherent optical DAC transmitter [4]. The power consumption of the transmitter primarily depends on the driver architecture. An efficient PIN-RC phase shifter contributes to achieving a small-size transmitter. Due to the combination of the efficient PIN-RC segmented modulator and 28-nm CMOS inverter driver, our transmitter realizes a highly power-efficiency and a compact size.

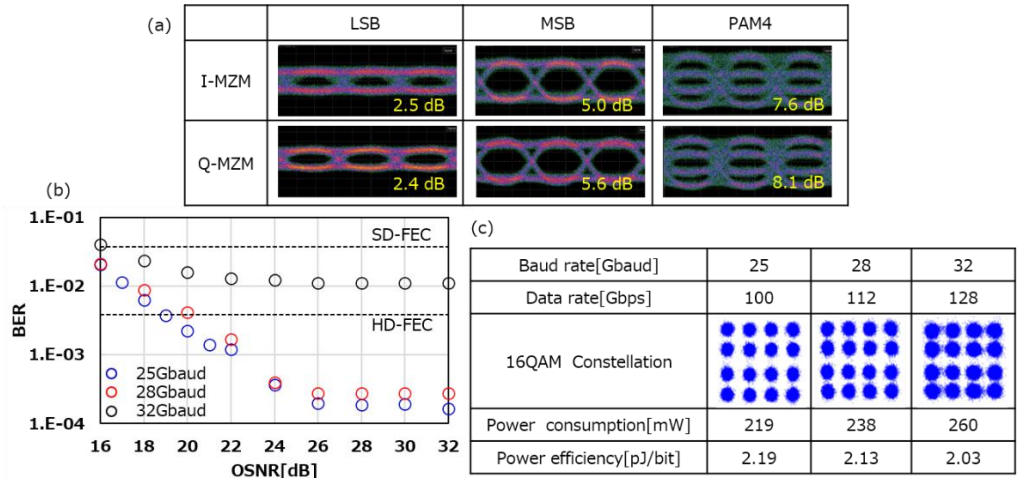

Fig. 3. (a) Output waveform and extinction ratio of each child-MZI. (b) BER vs. OSNR performance of the optical DAC transmitter. (c) 16QAM constellation and power efficiency of the optical DAC transmitter at 25–32 Gbaud.

4. Conclusion

An optical DAC transmitter integrated on an all-silicon segmented modulator and a CMOS inverter driver was experimentally tested. The transmitter demonstrated both high power-efficiency of 2 pJ/bit and low BER under SP 128G 16QAM operation. The optical DAC architecture employing a PIN-RC segmented modulator provides significant advantages in terms of its size, complexity, and power consumption without electrical DACs and linear drivers.

5. Acknowledgments

This paper is based on results obtained from a project, JPNP14004 and JPNP16007, commissioned by the New Energy and Industrial Technology Development Organization (NEDO).

6. References

[1] C. Doerr et al., "Silicon Photonics in Optical Coherent Systems," proc of IEEE, vol 106, pp. 2291-2301, 2018.
[2] T. Yamase, M. Sato, H. Noguchi, K. Sato, and T. Kato, "Low-power multi-level modulation of InP MZM with In-line centipede structure directly driven by CMOS iC," in *Proc. Opto. Electron. Commun. Conf.*, 2013, Paper WK2-3.
[3] X. Wu et al., "A 20Gb/s NRZ/PAM-4 1V transmitter in 40nm CMOS driving a si-photonic modulator in 0.13 μm CMOS," Int. Solid-State Circuits Conf. (ISSCC) 2013, pp. 128–130.
[4] A. Shastri, et al., "Ultra-Low-Power Single-Polarization QAM-16 Generation Without DAC Using a CMOS Photonics Based Segmented Modulator" J. Light Wave Technol., vol.33, no.6, pp.1255-1260, Mar. 2015.
[5] S. Tanaka, et al., "Ultralow-Power (1.59 mW/Gbps), 56-Gbps PAM4 Operation of Si Photonic Transmitter Integrating Segmented PIN Mach–Zehnder Modulator and 28-nm CMOS Driver" J. Light Wave Technol., vol.36, no.5, pp.1275-1280, Mar. 2018.
[6] Y. Sobu, et al., "High-Speed Optical Digital-to-Analog Converter Operation of Compact Two-Segment All-Silicon Mach–Zehnder Modulator" J. Light Wave Technol., vol.39, no.4, pp.1148-1154, Jan. 2021.