Development of Low-power Coherent ASIC

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Abstract: The latest generation of coherent pluggable modules impose strict power limits on the coherent ASIC. The development process for a low-power coherent ASIC designed in a 7nm FINFET process is described. The ASIC enables pluggable coherent modules with energy efficiency of 40-60pJ/bit for various 400G DWDM applications. © 2022

1. Introduction

The introduction of coherent optical communication technologies has played a key role in enabling the buildout of communication networks to meet increasing capacity demands which have transformed the daily lives of billions of people all over the world. Coherent optical systems *[1]* provide better spectral efficiency and enable the use of linear digital signal processing to compensate for optical fiber impairments compared to the prior intensity modulation approaches. These benefits have enabled the cost-effective deployment of optical links which span hundreds to thousands of kilometers with just optical amplification. The use of DWDM (dense wavelength division multiplexing) has pushed practical deployments on a single fiber pair to over 10Tbps in long-haul deployments and over 25Tbps in metro/regional deployments. The capacity of single coherent ports has increased to 400Gbps and beyond with the latest generation devices.

The latest generation of devices are enabling the deployment of speeds of 400Gbps in pluggable form factors (CFP2, QSFP-DD or OSFP) where power dissipation is a key concern. Pluggability has been key to increasing the density of these deployments with the capability to deploy as much as 12.8Tbps of capacity within a 1RU (rack-unit) switch/router. These developments have required the development of lower power and miniaturized electro-optical components and low power ASIC to perform the digital signal processing required in these modules *[2]*.

2. Requirements of a coherent ASIC

The low-power coherent ASIC is the key building block which interfaces with a framer or switch on the host side and the electro-optical components on the line side as shown in Figure 1. It performs the key functions of serializer/deserializer (SERDES), framing, encoding/decoding, digital signal processing and the digital-to-analog/analog-to-digital conversion (DAC/ADC). Table **1** summarizes the ASIC definition to enable a 400ZR standard interface [3]. A block diagram of a coherent ASIC is shown in Figure 2.

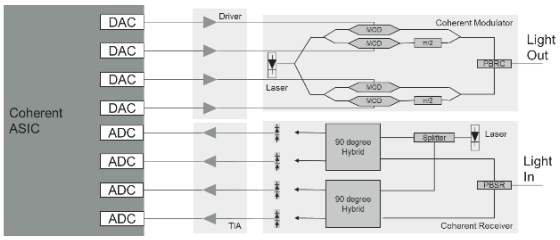

Figure 1: Block diagram of a coherent module

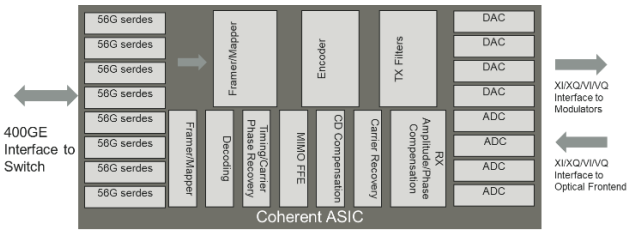

Figure 2: Block diagram of coherent ASIC

2.1. Analog Line Interface

A low-power coherent ASIC requires the use of low-power, high-bandwidth and high-sample rate analog converters to interface with the electro-optical components inside a coherent module. For example, to enable a 400ZR coherent interface, the ASIC needs four differential electrical interfaces capable of carrying the signals running at a 59.87GHz symbol rate. The analog front-end of the ASIC in 7nm FINFET technology was designed for nearly 40GHz bandwidth, sample rates as high as 97Gsamples/s with 8bit resolution and jitter less than 150fsrms [4]. These converters require less than 35fJ/conversion-step and represent a huge improvement over the state of the art. The entire analog front-end including the PLLs consumes less than 3W.

Table 1: Definition of an ASIC for 400ZR

Type of line interface	400ZR
Symbol rate of line interface	59.87GHz
Number of electrical lanes	4
Modulation of line interface	DP-QAM16
FEC of line interface	C-FEC with 15% overhead
Pilot overhead of line interface	3%
ROSNR Tolerance	26db
Chromatic Dispersion Tolerance	2400ps/nm
Type of Host interface	400GAUI-8
Number of host lanes	8
Symbol rate of host interface	26.5625GHz
Modulation of host interface	PAM4
FEC of host interface	RS(544,514)
Link Loss Budget	10.2db

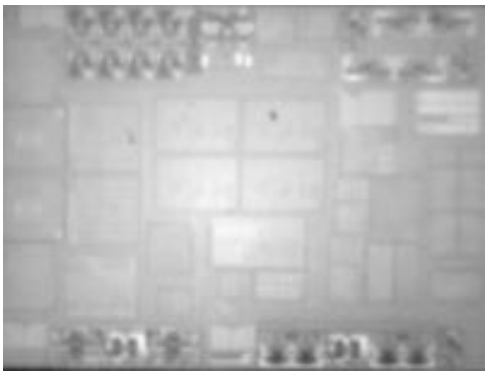

Figure 3: Die photo of an ASIC for 400G applications

2.2. Host Interface

The coherent ASIC consists of a host interface which is intended to transfer data to and from a framer or a switch ASIC over 8 differential electrical traces with a link loss less than 10.2db. Each lane of the host interface is a self-timed PAM4 serdes operating at a 26.5625GHz symbol rate. Each lane consists of an analog front-end with timing recovery, equalization and slicer functionality. These interfaces make use of extensive calibration to reduce power dissipation. The entire 400GAUI-8 interface is protected by a RS(544,514) forward-error correction code. The host interface is terminated within the coherent ASIC and the payload is mapped into the line-side frames. The eight lanes of the host interface are designed to be reconfigurable to support other ethernet and OTN interfaces such as 100GAUI-4, 100GAUI-2, 200GAUI-4, OTL4.4, and FOIC4.8, which are defined in various standards bodies [5] [6].

2.3. Framing

The framing functionality in the ASIC is intended to adapt the data from the host interface into frames suitable for the coherent line interface. Because of the geographically disperse nature of coherent networks, the interfaces typically need a lot of instrumentation to identify and locate faults. Standards bodies such as ITU-T have defined some of these frames and the extensive overhead information that needs to be added and processed for management, maintenance and fault-isolation purposes [6].

2.4. Transmit Digital Processing

The transmit digital implements the functions of FEC encoding, modulation and filters to shape the optical output signal spectrum. The transmit filters required for transmission are a function of the module driver and optical modulator designs and compensate for impairments such as a non-flat frequency response, reflections and non-linearity. The filters also shape the spectrum to minimize inter-channel interference in DWDM applications with close spacing of the wavelengths. Design of these digital blocks for low-power requires careful analysis of the filter length requirements, choice of filter architecture and optimization of bit-widths of the datapaths.

2.5. Receive Digital Signal Processing

The receive signal processing requires the most power intensive blocks in the coherent ASIC. Some key blocks required in the receiver are chromatic dispersion compensation, polarization mode dispersion (PMD) compensation, carrier phase and frequency recovery, timing recovery and equalization [7] [8]. Optimization of this block for power starts at the architectural stage with the choice of sampling rates to minimize the overall module power. The choice of oversampling also determines the optimal choice of parallelism of the digital datapaths. Due to the high symbol rates, the datapaths are parallel and process many symbol periods in each clock period. This parallel processing introduces latency which affects the signal processing algorithms when there are feedback loops which require fast tracking. Due to the lengths of the filters involved, frequency domain processing using FFT and overlap-save or overlap-discard architectures are commonly used for chromatic dispersion [8]. Choices such as the order of the signal processing blocks, equalizers, carrier recovery, and timing recovery impact the ability of the receiver to track time varying impairments and affect the overall power dissipation of the ASIC and the module.

2.6. Process Choice

Due to the high-speeds involved and low-power requirements, coherent ASICs can typically make use of the capabilities of the latest CMOS process node offered by the fabrication facility. Analog designs take advantage of the advanced process nodes by incorporating digital calibration techniques to ease the analog requirements. The

digital intensive nature of coherent ASICs allows the design to take advantage of the power savings from advanced nodes coupled with designs to take advantage of the higher speed devices available in the process to get a net reduction in energy per bit. Current generation devices are designed in 7nm FINFET process while newer generation devices are expected to be designed in 5nm or 3nm processes.

2.7. Adaptive Voltage Scaling (AVS)

To meet the demanding power requirements of a coherent ASIC, a closed loop adaptive voltage scaling system (AVS) is critical. It enables significant digital power reductions by eliminating regulator tolerances and minimizing power over the process manufacturing window and operating temperature range. Implementing a functional AVS scheme requires the measurement of process, voltage and temperature parameters on-chip and adjustment of the supply voltage to the optimal value based on these parameters. Implementing a functional AVS scheme requires an understanding of the CMOS process, the timing sign-off criteria and an understanding of the digital blocks on the chip.

3. Conclusion

A low-power coherent ASIC was developed in a 7nm FINFET process to enable 100/200/400G coherent pluggable modules for DWDM applications. These modules in form-factors such as QSFP-DD, OSFP and CFP2 achieve energy efficiencies from 40-60pJ/bit depending on the application. Figure 3 shows a die photograph of this chip. The future coherent systems will require even higher symbol rates to enable higher speed interfaces for DWDM networks. In addition, coherent interfaces are expected to be used for shorter reaches on unamplified links as the prior approaches reach their limits *[9]*. These interfaces require development of even lower power coherent ASICs to meet the power limits of next generation modules.

Acknowledgement

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