Terabit Transmitters Using Heterogeneous III-V/Si Photonic Integrated Circuits

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Abstract: Heterogeneous photonic integrated circuits are being demonstrated with Tbps capacity and higher performance, with laser linewidths below 1 kHz and volumes scaled to multimillion per annum production levels. © 2020 John Bowers

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Hyperscale data centers (HDCs) are growing rapidly and driving Internet traffic to an astounding 20 zettabytes by 2021 [1]. HDCs are expected to drive switch ASICs to scale from 25 Tbps today in 2020 to 50 Tbps in 2022 and 100 Tbps in 2025. This drives transceiver data rates to 800 Gbit/s by 2024. Further, the need for higher capacity and lower IO power drives the integration of PICs into EIC packages in 2022 and drives 3D EIC PIC integration. This allows the elimination of power-hungry electronics such as those associated with equalization, clock recovery, DSP or high bandwidth optical- and electronic- phase locked loops [2].

Fortunately, a number of innovations make this possible. Progress in silicon photonics and in laser integration into heterogeneous Si PICs has enabled rapid volume scaling of Si PICs to multimillion transceiver run rates in just a few years [3]. Second, the low loss of silicon and silicon nitride waveguides has enabled resonators with Qs of 10^8 or more along with heterogeneous Si lasers with linewidths under 1 kHz (Fig. 1ab) [4]. Furthermore, the use of quantum dot (QD) active regions enables high performance mode locked lasers for DWDM comb sources, reducing power and layout size for transceivers with tens or hundreds of lines [5]. QD active regions also allow for reduced reflection sensitivity and enable PIC integration without optical isolators [6]. One can envisage using these DWDM sources for high speed low energy consumption datacenter interconnects which will require 0.1 pJ/bit power consumption and 5 Tbps/mm^2 bandwidth density. Such interconnects will require using the latest advancements (e.g. TSVs and TOVs) in CMOS processing for flip chip integration of electronic drivers and control circuitry on the silicon PIC (Fig. 1c).

Transitioning these innovations to silicon photonics foundries is ongoing [7] and is promising for continued rapid advances on optical transceivers, high capacity switches, memory and processors.

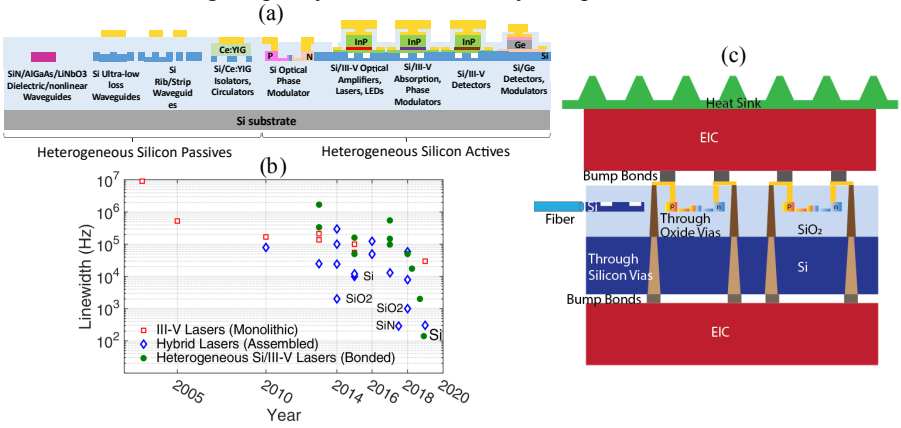

Fig. 1 (a) The heterogeneous silicon platform has flexibility to incorporate III-V and otherwise incompatible materials onto 300mm silicon wafers. Device performance can be optimized without sacrificing the potential for scalability. (b) Comparison of semiconductor laser linewidths using different integration approaches and (c) schematic diagram of a high-density low energy consumption EIC-PIC datacenter transceiver

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[1] Cisco Systems "Cisco Visual Networking Index: Forecast and Trends, 2017–2022 White Paper," *Cisco Forecast*
[2] D. J. Blumenthal *et al.*, *2019 8th Annu. IEEE Photonics Soc. Opt. Interconnects Conf. OI 2019*, pp. 1–2, 2019
[3] R. Jones *et al.*, "Heterogeneously Integrated Photonics", IEEE Nanotechnology Magazine 17, April (2019).
[4] M. A. Tran et al., "Tutorial on Si/III-V Heterogeneous Integration for Narrow Linewidth Semicond. Lasers", APL Photonics **4**, 111101 (2019).
[5] S. Liu, et al., "High-channel-count low-noise 20 GHz passively mode locked quantum dot laser directly grown on Si with 4.1 Tbit/s transmission capacity", Optica 6(2), 128 (2019).
[6] J. Duan *et al.*, "1.3-um Reflection Insensitive InAs/GaAs Quantum Dot Lasers Directly Grown on Silicon", IEEE PTL 31(5) 345, (2019).
[7] R. Helkey *et al.*, "High Performance Photonic Integrated Circuits on Silicon", IEEE JSTQE 25, 8300215, (2019)