A 0.57-mW/Gbps, 2ch x 53-Gbps Low-Power PAM4 Transmitter Front-End Flip-Chip-Bonded 1.3-μm LD-Array-on-Si

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Abstract: A low-power 2-channel PAM4 transmitter front-end consisting of 65-nm CMOS PAM4 shunt LD drivers and flip-chip-bonded 1.3-μm LD-array-on-Si achieves simultaneous 2ch x 53-Gps PAM4 transmission over 2-km-long SSMF with power efficiency of 0.57 mW/Gbps. © 2020 The Author(s)

1. Introduction

Ethernet transmission capacity has grown rapidly. Corresponding to its rapid growth, the standard for 400GbE has already been established. In the future, discussions of the standard for 800G/1TbE will start. Four-level pulse amplitude modulation (PAM4), a key modulation technology for 400 GbE, will be important for 800G/1TbE. In addition, for 400GbE, 800G/1TbE and beyond, low-power-consumption technology is important. The conventional PAM4 transmitter front-end uses a digital-to-analog converter (DAC) and linear driver. The DAC generates a PAM4 signal, and the linear driver amplifies it to drive an LD. Recently, to decrease power consumption of the transmitter front-end, PAM4 drivers with DAC functions but without a linear driver have been reported [1–6]. As a low-power NRZ transmitter front-end, we have demonstrated a 4 ch x 25-Gbps NRZ transmitter front-end consisting of shunt LD drivers and flip-chip-bonded LD array [7]. Since the shunt LD driver is placed in parallel with an LD without impedance matching, the transmitter front-end using the shunt LD driver is a low-power architecture. To avoid multiple reflections due to impedance mismatch, the flip-chip-bonding interconnection technique, which can minimize multiple reflections, is needed for the transmitter front-end. However, a PAM4 driver using the shunt LD driver architecture and flip-chip-bonding interconnection technique have not yet been reported.

In this work, we devised a low-power 2-channel PAM4 transmitter front-end consisting of a 2-channel 65-nm CMOS PAM4 shunt LD driver and flip-chip-bonded 1.3-μm LD-array-on-Si. Each channel operates simultaneously with 53-Gbps PAM4 signals, resulting in record power efficiency of 0.57 mW/Gbps. Clear digitally interpolated 53-Gbps PAM4 eye diagrams after 2-km standard single-mode fiber (SSMF) transmission were observed in simultaneous 2-channel operation using offline feed-forward equalization (FFE). The bit error rate (BER) was below 2.3×10^{-4} with both channels operating simultaneously over 2-km-long SSMF.

2. Structure of low-power 2-channel PAM4 transmitter front-end

Fig. 1(a) shows a block diagram of the 2-channel PAM4 transmitter front-end. The dashed line outlines the 2-channel driver IC. Each driver uses the CMOS PAM4 shunt LD driver architecture. The PAM4 driver consists of two core parts and two equalizing parts on the least significant bit (LSB) and most significant bit (MSB) sides. The core parts consist of NMOS transistor M_1 and M_3, PMOS transistor M_2 and M_4, and resistors. The equalizing parts consist of capacitors and resistors. V_1 and V_4 are supply voltages, and V_2 is the gate bias voltage of M_1 and M_2. V_3 is the gate bias voltage of M_3 and M_4. Since the operating voltage of M_1 and M_3 is lower than that of the LD, the offset voltage V_4 can be set so that the power consumption of the PAM4 shunt LD driver is decreased. In addition, V_1, V_2, V_3, and V_4 are common voltages between both channels. The anode and cathode terminals of the LD are connected to the output terminals of the driver, V_{outa} and V_{outc}, by flip-chip bonding, respectively. V_{outc}, which is connected to the ground lines inside the PAM4 driver IC, is connected to the ground terminal outside the PAM4 driver IC by wire bonding. The parasitic inductance of the flip-chip bonding wire is denoted as L_{FCW}. LD current and shunt driving currents for each channel are denoted as I_{LD} and I_{DRVN1}, I_{DRVP2}, I_{DRVN3}, and, I_{DRVP4}, respectively. I_{LD} equals I_{DRVP2} minus I_{DRVN1} plus I_{DRVP4} minus I_{DRVN3}. For modulating I_{LD} in 53-Gbps PAM4, 26.5-Gbps NRZ signals are input into the LSB and MSB sides. Fig. 1(b) shows the operation of core parts. I_{DRVP} supplies bias current and modulation current to the LD, and I_{DRVN} supplies modulation current to the LD. I_{DRVN} is proportional to the input signal V_{in}, but the logic of I_{DRVP} and I_{LD} is inverted logic of V_{in}. When V_{in} is high, M_1 and M_2 are in the on- and off-state,

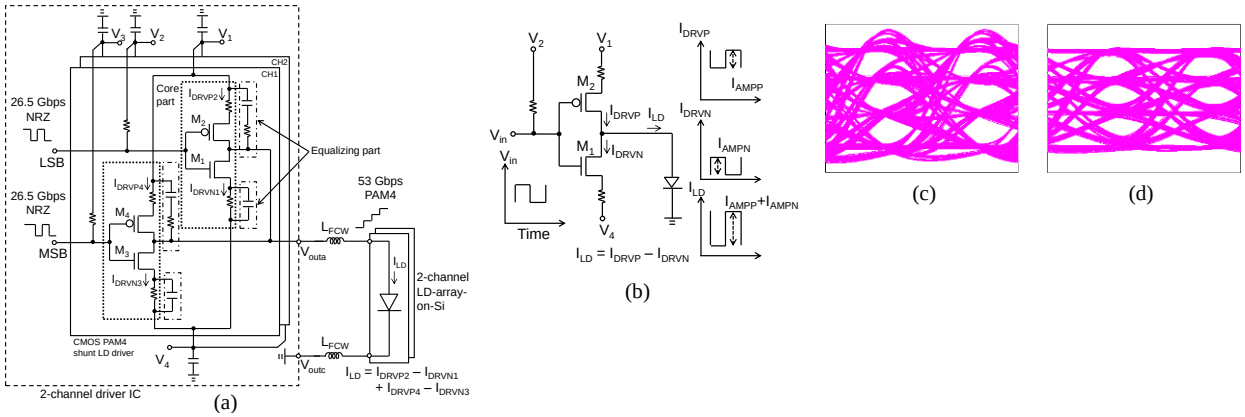

Fig. 1. (a) Block diagram of 2-channel PAM4 transmitter front-end. (b) Operation of core parts. Simulated 53-Gbps/ch PAM4 optical output waveform for simultaneous operation (c) without equalizing part and (d) with equalizing part.

respectively, and I_{DRVN} and I_{DRVP} are high and low, respectively. Therefore, I_{LD} is low. When V_{in} is low, M_1 and M_2 are in the off- and on-state, respectively, and, I_{DRVN} and I_{DRVP} are low and high, respectively. Therefore, I_{LD} is high. Since I_{LD} equals I_{DRVP} minus I_{DRVN}, the amplitude of I_{LD} equals the amplitude of I_{DRVP}, $I_{AMPP,}$ plus the amplitude of I_{DRVN}, I_{AMPN}. Compared with our previous driver [7], since our new CMOS PAM4 shunt LD driver does not use PMOS transistors as sources of constant current, but for modulation functions, this driver has a low-power architecture and operates with low input signal amplitude. Fig. 1(c) and (d) show simulated 53-Gbps/ch PAM4 optical output waveforms for simultaneous operation without and with the equalizing part, respectively. We configured equivalent circuit models of the LD and rate equations in our HSPICE environment to simulate the electric-optic conversion behavior [8]. As shown in Fig. 1(a), (c), and (d), the equalizing part consisting of RC filter on the M_2 side suppresses overshoot of PAM4 optical waveforms. In addition, the equalizing part consisting of a capacitor on the M_1 side decreases the fall time of PAM4 optical waveforms.

Fig. 2 shows microphotographs of the 2-channel PAM4 transmitter front-end, 2-channel membrane LD-array-on-Si, integrated with a spot-size convertor (SSC) [9], and 2-channel PAM4 driver IC. In the driver IC, the left and right pads of channel 1 and 2 are V_{outc} and V_{outa}, respectively. The ground pads of the 2-channel driver IC are connected to the ground terminal through the GND posts by wire bonding. LSB_1 and MSB_1 are input terminals for channel 1; LSB_2 and MSB_2 are those for channel 2. The driver IC chip was fabricated in 65-nm CMOS technology. Dummy pads, which the dashed line outlines, are used to prevent the 2-channel LD-array-on-Si from leaning when the LD array is flip-chip bonded to the driver IC. The face-down LD array is stably connected to the driver IC by flip-chip bonding through Au bumps bonded to V_{outc}, V_{outa}, and the dummy pads. V_{outa} and V_{outc} of the driver are connected to the p and n terminals of the LD array, respectively. The flip-chip bonding interconnection technique minimizes the parasitic inductance between the LD array and driver IC. Therefore, bandwidth degradation due to bonding interconnections is suppressed.

3. Measurement results

We measured the BER performance for discrete and simultaneous operation of the 2 channels with 53-Gbps PAM4 signal after 2-km transmission using SSMF. Lasing wavelengths were 1296–1300 nm. The 26.5-Gbps NRZ pseudo-random bit sequence signals with a word length of 2^{15}-1 from the pulse pattern generator were input into both the LSB and MSB sides of the 2-channel PAM4 driver with RF probes. The input signal amplitude was 0.3 V_{pp}. The LD bias current of channels 1 and 2 was set to 9.9 mA. The measurement was carried out via a single-mode high-numerical-aperture fiber that was butt-coupled with the SSC on the LD chip and was spliced to SSMF at the opposite side. The optical PAM4 signals from the LD chip were measured through 2-km-long SSMF and a variable optical attenuator. To measure the BER, we used a receiver (DSC-R409, Discovery Semiconductors, Inc.) consisting of a photodiode and transimpedance amplifier. Received signals were acquired with a digital storage oscilloscope with a 20-GHz analog bandwidth and 50-GS/s sample rate. We demodulated the received signals with offline digital signal processing, where we used adaptive FFE. Fig. 3 shows 2-channel digitally interpolated 2-km-transmission 53-Gbps/ch PAM4 eye diagrams of the received signal after the offline FFE with 17 taps. The PAM4 eye diagrams of both channels have equally spaced and clear eye openings. Fig. 4 shows the measured BER dependence of received power for discrete and simultaneous operation over 2-km-long SSMF. The crosstalk penalties between discrete and simultaneous operation are negligible in both channels. The BER at 2-km SSMF output of channels 1 and 2 are below 2.3×10^{-4}, assuming 5.8% overhead RS (544, 514) FEC [10]. At a BER of 2.3×10^{-4}, the minimum receiver sensitivities of channels 1 and 2 for 2-km transmission are -3.3 and -3.1 dBm, respectively. The power margins of

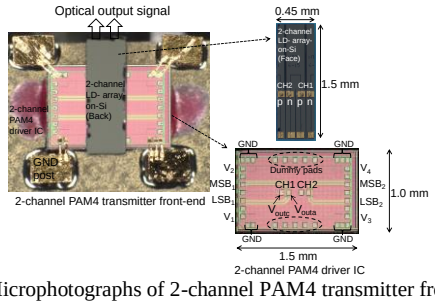

Fig. 2. Microphotographs of 2-channel PAM4 transmitter front-end (left) and the 2-channel LD-array-on-Si and 2-channel PAM4 driver IC (right).

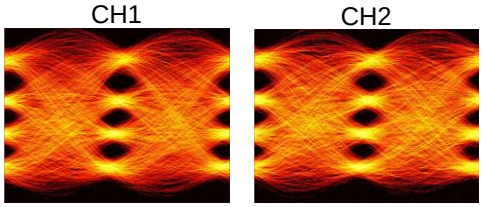

Fig. 3. 2km-transmission 53-Gbps/ch PAM4 eye diagrams after FFE.

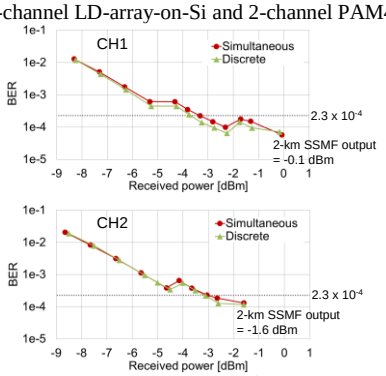

Fig. 4. Measured BER dependence of received power for discrete and simultaneous operation over 2-km-long SSMF.

Table 1. Comparison of state-of-the-art low-power PAM4 transmitter front-ends for DFB-LD and VCSEL optical transmission systems

		[6]	[5]	[4]	[3]	[2]	[1]	This work
IC technology		0.13-μm SiGe BiCMOS	0.25-μm InP DHBT	0.13-μm SiGe BiCMOS	90-nm CMOS	90-nm CMOS	65-nm CMOS	65-nm CMOS
LD technology		VCSEL	850-nm VCSEL	VCSEL	VCSEL	VCSEL	VCSEL	1.3-μm DFB-LD
Chip mounting technology		Wire bonding	Wire bonding	Wire bonding	-	-	-	Flip-chip bonding
Single data rate [Gbps]		90	56	56	25	20	56	53
Channels		1	1	1	1	1	1	**2**
Total data rate [Gbps]		90	56	56	25	20	56	106
Power consumption [mW/ch]	Driver	-	183	97.2	87.47	34.1	32	**13.4**
	Driver and LD	177	207	115	-	-	-	**30.3**
FOM [mW/Gbps/ch]	Driver	-	3.27	1.74	3.50	1.71	0.56	**0.25**
	Driver and LD	1.97	3.70	2.05	-	-	-	**0.57**
Bit error rate		- (PRBS7)	$<10^{-12}$ (PRBS7)	- (PRBS9)	-	-	-	$<2.3 \times 10^{-4}$ (PRBS15)
Transmission length		-	BtB	-	-	-	-	**2 km**

channels 1 and 2 are 3.2 and 1.5 dB, respectively. These results show that we successfully transmitted 2ch x 53-Gbps PAM4 optical signals for simultaneous and discrete operation over a distance of 2 km without an optical amplifier. The total power consumption of the 2-channel PAM4 transmitter front-end, including the 2-channel PAM4 driver and LD array, is only 60.7 mW, resulting in 0.57 mW/Gbps.

Table 1 compares our 2-channel PAM4 transmitter front-end with state-of-the-art low-power PAM4 transmitter front-ends designed for DFB-LD and VCSEL optical transmission systems. Refs. [1]–[3] reported only simulation results. The figure of merit (FOM) is defined as power consumption divided by single data rate. The FOMs of our 2-channel PAM4 driver, 0.25 mW/Gbps/ch, and transmitter front-end including an LD array, 0.57 mW/Gbps/ch, are the lowest in the table.

4. Conclusion

We have devised a low-power 2-channel PAM4 transmitter front-end consisting of a 2-channel 65-nm CMOS PAM4 shunt LD driver and flip-chip-bonded 1.3-μm directly modulated LD-array-on-Si. Each channel of the transmitter front-end operates simultaneously with 53-Gbps PAM4 signal, resulting in power efficiency of 0.57 mW/Gbps. A 2-km-long SSMF transmission with 53-Gbps PAM4 signal, with the 2-channel transmitter operated simultaneously, was successfully demonstrated with a BER below 2.3×10^{-4}. To the best of our knowledge, our 2-channel PAM4 transmitter front-end achieves the best power efficiency among reported PAM4 transmitter front-ends. This transmitter suggests the feasibility of transmission over a distance of 10 km with a low-power architecture.

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