Reliability Failure Modes of an Integrated Ge Photodiode for Si Photonics

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Abstract: Major failure modes of Germanium photodiodes are proposed with a model. These are: catastrophic breakdown driven by thermal runaway due to localized self-heating and electrical defect generation/activation driven by electric field with photocurrent localization effect. © 2020 The Authors

1. Device Structure

The Ge-on-Si waveguide vertical PIN photodetectors were fabricated on a 300 mm SOI wafer with 120 nm silicon layer on 2 μm buried oxide. (Fig. 1A) The undoped germanium absorption layer was grown on top of a p-type doped silicon waveguide, and an n+ type dopant implanted. Ohmic contacts and metal routing were formed to both the p-type Si waveguide layer on the side of the device and the top n+ Ge layer. The light propagating in the silicon waveguide is directly coupled into the upper Ge layer deposited on top of the Si layer, where it is absorbed in the intrinsic layer of the PIN structure. A top-down view of the device layout is shown on Figure 1B.

Fig. 1A. Schematic Device Structure (cross-section)

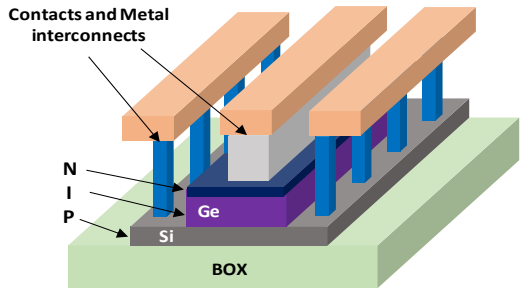
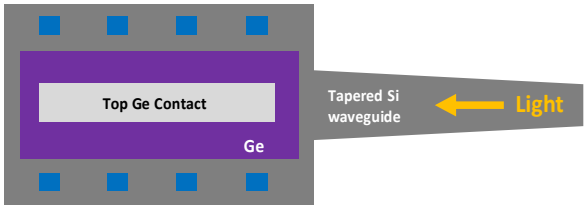


Fig. 1B. Device Layout



2. Thermal Runaway

2.1 Introduction

Several authors have described a thermal runaway mechanism in photodiodes which leads to catastrophic device failure [1-4]. In O-band (1310nm), incident light will be absorbed in a few microns in Ge. [5, 6] The total power (optical power plus electrical power) contributes to a highly localized self-heating. The total diode current is composed of two components- the induced photocurrent, which will be a weak function of temperature, and a "dark" current, which will be thermally activated, and a strong function of temperature. A rise in local temperature caused by a high photocurrent will cause the dark current to increase locally, which in turn raises the local temperature. In this paper, we introduce a positive feedback loop, resulting in a thermal runaway and device breakdown at a critical temperature T_{crit}.

2.2 Stress Methodology

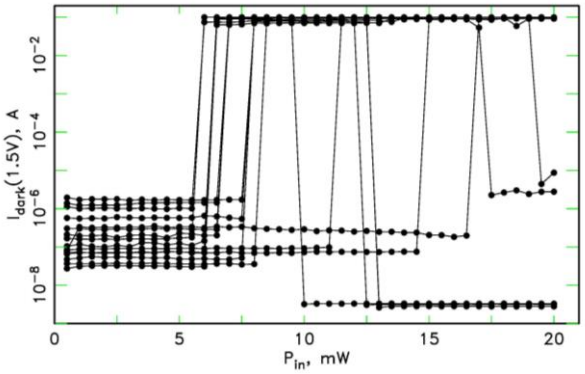
In order to characterize thermal overload failure, we performed optical power step stresses at wafer level. The stress voltage was fixed at V_{STR} = 8V (reverse bias), but the optical power input, P_{in}, to the test structure through a grating coupler was increased in constant steps. The variation in slope was dominated by variation in the optical coupling constant of the input grating. This was compensated for by using the readout photocurrent at -1V bias, $I_{RO.}$

2.3 Results

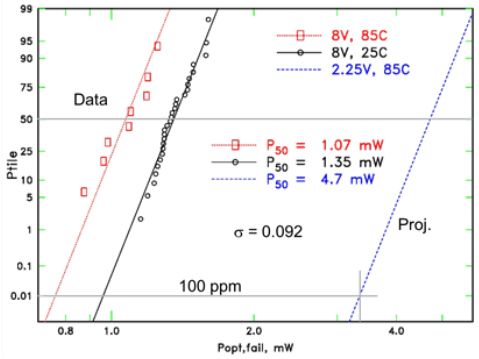
The dark current at -1.5V measured after each stress interval (see Figure 2A) clearly showed sudden device breakdown. After breakdown, current was at or very close to the external compliance limit of 100 mA. The stress current (I_{str}) is not linearly increased with optical power and initial slope of I_{str} is higher than the I_{RO} due to the avalanche multiplication factor M. As the power increases, there is excess current, I_x above the linear response, due

to the rise of local temperature and the non-optical current components. The total device power P_{tot} is: $P_{tot} = P_{opt} + I_{Str}V_{str}$. We define an effective temperature: $T_{eff} = T_A + \theta(P_{tot} + VI_{tot})$ and θ can be determined from the difference in P_{fail} between T_A = 25 and 85°C. From an Arrhenius plot (now shown here) of I_x vs T_{eff}, activation energy (E_a) and I_0 can be extracted. When the photo diode is in reverse bias condition with optical power, total current is composed of generation current (I_{gen}), photo-current (I_{ph}) and diffusion current (I_{diff}). If we assume the diffusion current dominates the runaway, thermal runaway will occur when temperature reaches a critical values (T_{crit}). The model prediction is compared with experimental results and the agreement is good. The distributions of estimated $P_{opt,fail}$ are plotted in Figure 2B, fit to log normal distributions with a common sigma of 0.092. For a Cumulative Failure Rate (CFR) = 100 ppm, the maximum P_{opt} is estimated to 3.3 mW.

Fig. 2A. I_{dark} readout measurements at 1.5V at each step



2B. Projection of $P_{opt.fail}$ stastics to use condition



3. Defect Generated Dark Current Degradation

3.1 Introduction

The dark current gradual shift at Ge photo-detector (PD) due to stress under electrical bias has also been reported in the literature [5]. The interface between Ge PD and Si substrate which has hetero-junction needs to be characterized under electrical and optical stress conditions, and the interface property change can be a cause of the dark current shift. Ideality factor extraction from dark I-V at forward bias region can give us important information about the junction characteristic [6]. In this paper, the interface quality between Ge and Si is investigated by utilizing the ideality factor shift of stressed device.

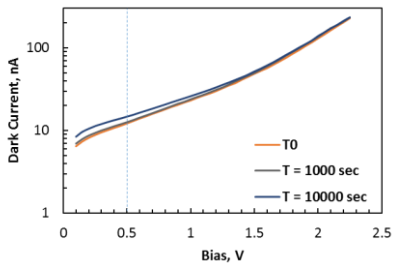
3.2 Stress Methodology

The devices were stressed at wafer level with constant reverse bias and no light input for electrical stress only. The stress conditions were: V_{STR} = 8V, T_A = 30ºC. Periodic measurements of dark current I-V curves were done. Electrical/Optical stress was given to the other set of devices. V_{STR} = 8V, P_{IN} = 4mW, T_A = 30ºC. Periodic measurement is same with electrical stress only case.

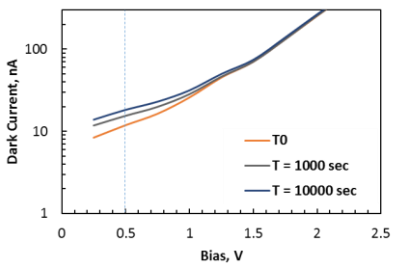
3.3 Results

Dark I-V under electrical stress only and electrical/optical stress are shown in Figure 3A and 3B. The device with electrical/optical stress has a significant increase of dark current level at -0.5V compared to the device with electrical stress only. Dark current shift (see Figure 3C) at electrical/optical stress shows significant higher (~10x) than electrical stress only. Optical stress is enhancing the degradation of junction leakage

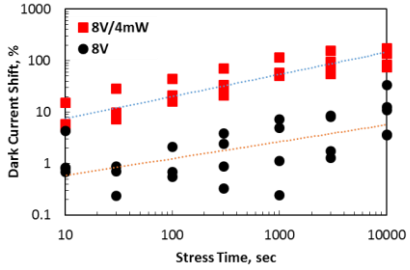
Fig. 3A. Dark I-V under 8V stress



3B. Dark I-V with 8V/4mW stress



3C. Dark current shift comparison

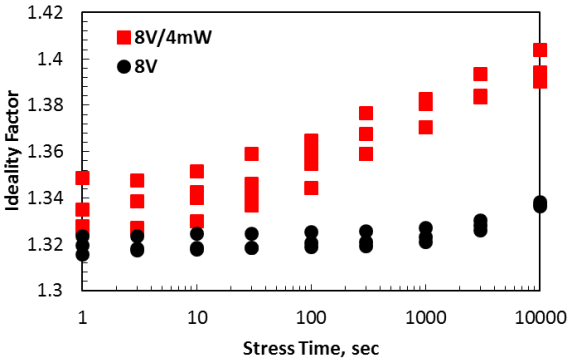


Ideality factors are extracted from dark I-V equation. In the dark condition, the current level is less than 10^{-6} ampere (A) range, so voltage drop by series resistance can be negligible. To extract reasonable ideality factor, the shunt resistance (R_{sh}) which means the resistance of physical path at junction should be larger than 2000 mA/cm^2 [7]. The extracted R_{sh} in this study are all higher than the bottom limit so R_{sh} term at right side also can be ignorable.

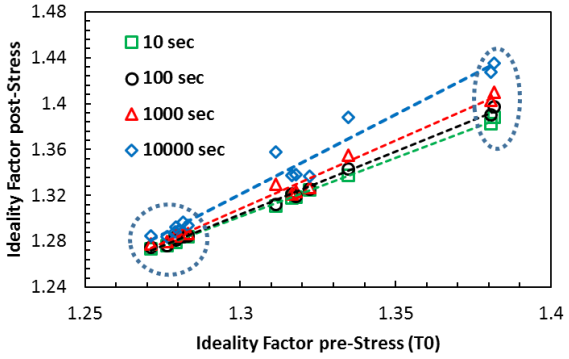
$$I = I_0\left\{exp\left[\frac{q(V-IR_s)}{nkT}\right]-1\right\}+\frac{q(V-IR_s)}{R_{sh}}$$

Figure 4A shows the ideality factor variation with stress time. Compared to the electrical stress only case, optical/electrical stress shows an increase of ideality factor after 10 seconds which means the recombination at junction interface is more dominant than the bulk Ge layer as the optical stress is added to the electrical stress. The gap of ideality factors between two stress groups is wider as stress time increases. It means the optical stresses promote the enhancement of defect generation at the junction area and the degradation of interface quality. This result is consistent with the dark current shift in Fig. 3C. We investigate the initial interface condition effects on the interface degradation (shown in Figure 4B). The ideality factor variation between pre-stress and post-stress is very small or negligible for the devices having low pre-stress ideality factor, however, the devices with high ideality factor at pre-stress show significant increase of ideality factor after stress. It explains that the initial interface condition has an important role at degradation under optical stress. Since Ge and Si have 4.18% of lattice misfit and 100% Ge layer on Si has 3~4nm of critical thickness [8]. So high-quality initial Ge layer on Si can reduce the degradation of the interface by optical stress in silicon photonics technology

Fig. 4A. Extracted ideality factor after stress



4B. Ideality factor comparison, pre-stress vs post-stress



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