1.52 Tb/s single carrier transmission supported by a 128 GSa/s SiGe DAC

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Abstract: We report on a new 128 GSa/s SiGe digital to analog converter supporting data generation at 128 GBaud. We demonstrate successful transmission at 1.55 Tb/s net rate in back to back and 1.52 Tb/s after 80 km of SMF. © OFC 2020 The Authors.

1. Introduction

Coherent transmission systems require digital to analog converters (DAC) sampling at ever faster rates to generate signals at the transmitter of increasingly finer granularity and higher symbol rates. The sampling rates of DACs have reached 100 GSa/s for technologies based on Silicon-Germanium (SiGe) [1,2] and 120 GSa/s for CMOS-based converters [3,4]. Using them, the highest reported symbol rates lie in the vicinity of 100-105 GBaud. One way to increase the bitrate of an optical communication system is to increase the symbol rate, itself requiring an increase of the sampling rate of the underlying hardware – the DAC. Although solutions requiring a single DAC per dimension are preferred, the analog multiplexing (AMUX) of DACs is another way to increase the sampling rate [6-9]. As an example, the AMUX of 2 DACs was reported in [8] with sampling rates of up to 168 GSa/s. However, using 2 DACs and an AMUX to modulate a single dimension of an optical signal may also degrade its integrity and is less optimum with respect to cost, footprint and power consumption. A recent optical transmission experiment employing a single DAC per modulated dimension reported a net information rate (IR) of 6.5 bit per symbol per polarization [2]. A further increase of this rate is limited by the physical properties of transponders, such as their inherent maximum signal-to-noise ratio (SNR). Fig. 1 summarizes recent records for single carrier experiments at bit rates ≥1 Tb/s. The open circles '○'show data for transmitters using more than one DAC per dimension, while filled circles '●' show experiments using one DAC per dimension. Back-to-back (B2B) experiments are shown in grey. Multi-DAC-per-dimension solutions demonstrate that high bit rates can indeed be achieved by pushing up symbol rates, at the expense of a reduced signal integrity and thus reduced achievable information rate.

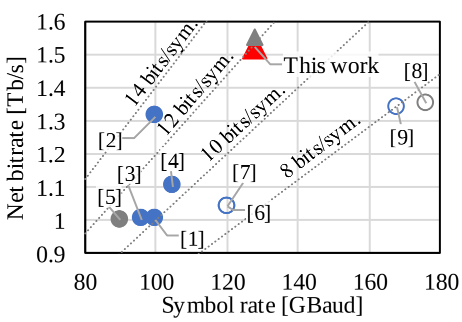

Fig. 1. Net bitrates versus symbol rate for recent record experiments 1 Tb/s. The dotted lines show thresholds of constant net information rates for polarization multiplex.

In this paper we present a new DAC implemented in SiGe technology with a maximum sampling rate of 128 GSa/s and 8 bits of nominal resolution. We report details of the converter implementation and its basic characterization regarding bandwidth and effective number of bits of resolution, and compare specification methods based on sinewave synthesis and broadband signal measurements. Finally, we assess the performance of the device in a coherent transmission system and report new net bit rate records for an optical transmission system utilizing a single optical carrier delivering 1.55 Tb/s in B2B and 1.52 Tb/s after transmission over 80 km of standard single mode fiber (SMF) with EDFA amplification. These achievements are also marked in Fig. 1 by triangles, outperforming previous records.

2. 128 GSa/s DAC and its assessment

The DAC prototype reported herein, called 'DAC5', was designed and manufactured by Micram and realized in STMicroelectronics's BiCMOS055 technology featuring high-speed bipolar transistors (f_T=325 GHz, f_{max}=375 GHz) combined with a 55 nm CMOS process on a 12″-wafer platform. The dies of area 6.04 x 5.14 mm² are mounted using wedge bonding to a RT/duroid□ 5880 high frequency laminate connecting the high-speed signals to coaxial 1.85 mm connectors (cf. Fig. 2a). The total power consumption of the module is typically 18 W per DAC at 128 GSa/s.

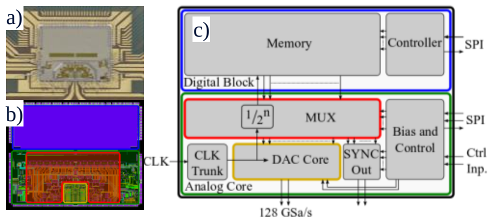

Fig. 2. a) Chip photography, b) chip layout and c) block description of the DAC5.

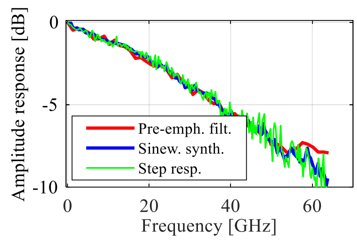

Fig. 3. Amplitude response derived by sinewave synthesis, step response and by pre-emphasis filter optimization.

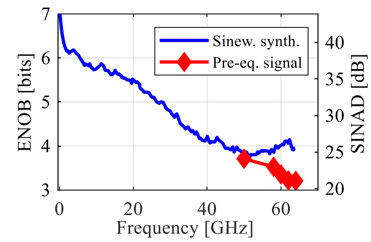

Fig. 4. ENOB vs. frequency derived by sinewave synthesis and SINAD for pre-eq. data at variable symbol rate.

Almost half of the chip area is occupied by a digital block containing the SRAM memory from which the digital payload of up to 512 kSamples is played back (Fig. 2b). Various hard coded test signals including PRBS sequences can be directly generated within this block. At the output of the digital block the data is fed to a 256:1 serializer which generates the 128 Gb/s data streams. In the DAC core these streams are converted to the analog output signal of 8 bits nominal resolution. An additional 128 Gb/s NRZ data stream is also generated by the serializer and fed to a different RF output to be used for other functions such as triggering test and measurements equipment. The selection of the hard-coded PRBS, the loading of an arbitrary data patterns to the memory and the calibration and optimization of the internal operating points are all controlled via an integrated SPI interface (see Fig. 2c). The DAC modules are controlled from a PC using a Python API connected via Ethernet to an on-board computer running a Linux firmware. The DAC5 supports a continuously adjustable sampling rate of up to 128 GSa/s which is controlled via the frequency of the half-rate clock applied to the device. Results of a sinewave synthesis at 128 GSa/s as defined per IEEE-1658 standard show a smooth frequency roll-off reaching 3 dB at 24 GHz, 6 dB at 43 GHz and eventually 10 dB at 64 GHz which represents the end of the first Nyquist band (cf. Fig. 3). In contrast to the 3 dB-bandwidth typically used as a figure of merit (FOM), the attenuation at the end of the first Nyquist band is the most relevant FOM for DAC-enabled communication systems as it determines the magnitude of the required pre-compensation filter when generating signals at one sample per symbol, i.e. at the highest symbol rate. The pre-compensation filter obtained by least mean squares adaptation is in good agreement with the measured frequency responses derived from both the step response and the response of sinewave syntheses. The effective number of bits (ENOB) measurements (where $ENOB_{[bit]} = (SINAD_{[dB]} - 1.76) \div 6.02$; and SINAD the signal to noise and distortion ratio) of the DAC, shown in Fig. 4, reveals the good linearity and the low noise of the converter. At low frequencies the DAC exhibits an ENOB of up to 6 bits while at frequencies close to Nyquist the ENOB falls to values between 3.8 to 4 bits. For the differential DAC output the ENOB is roughly 0.2 bit higher. We also measured the SINAD of pre-equalized PAM2 signals at symbol rates from 100 to 128 GBaud, as depicted by the red diamond markers in Fig. 4, resulting in slightly lower values than those from sinewave syntheses. Note that the effective amplitude of the pre-equalized data signal is symbol rate dependent and is up to 20% lower compared to a full-scale sine signal due to the FIR pre-emphasis.

3. System setup

The system setup is shown in Fig. 5. The data signal is generated by 2 SiGe DACs mounted on both sides of a common main board, sampling at 128 GSa/s and operating at 1 sample per symbol (cf. Fig. 5a). This mechanical arrangement minimizes the distance between both DAC outputs and allows for very short interconnects to the subsequent device. The DAC outputs are amplified (SHF S804B) and applied to a single-polarization $LiNbO_3$ IQ modulator having 45-GHz bandwidth, fed by a <100 kHz linewidth external cavity laser (ECL). Polarization multiplexing is emulated by a

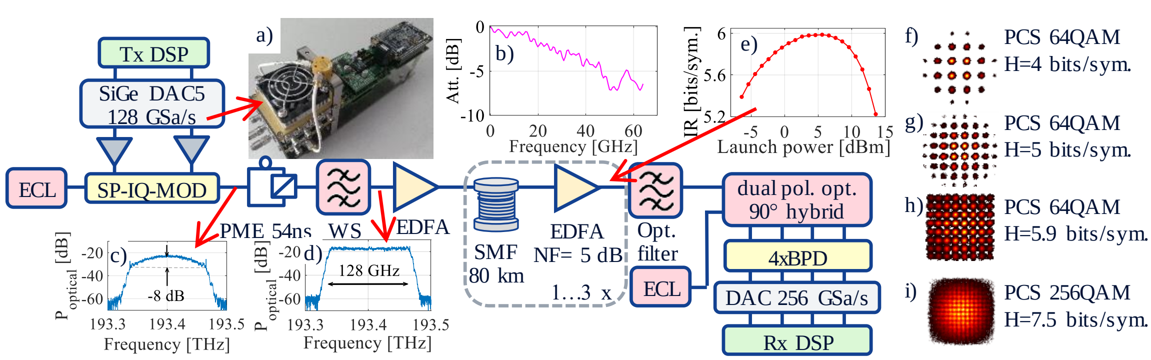

Fig. 5. Experimental setup. The insets show a) the DAC module photography, b) the frequency response of the pre-emphasis, c) the optical spectra after modulation, d) the optical spectra after optical filtering, e) the information rate versus launch power for SMF transmission at H=7.5 bits/symbol and f)-i) the scatter plots of mainly used PCS formats.

54-ns delay and add stage. The transmit digital signal processing (DSP) consists of a linear pre-emphasis filter to compensate for the combined DAC and driver responses (Fig. 5b), while the response of the modulator is compensated by an optical filter (Waveshaper – WS) which flattens the power spectral density (Fig. 5c) and d)) out of the IQ modulator. At the receiver the signal is amplified, filtered and applied to an optical 90° hybrid followed by balanced photodiodes (BPD) of 100 GHz bandwidth. The four resulting waveforms are acquired by a 80 GHz, 256 GSa/s real time oscilloscope. State of the art receiver-side DSP is performed off-line. Both the generalized mutual information (GMI) and the maximum net rate after successful FEC decoding are used as performance metrics. The transmission system is assessed both in B2B and over several spans of 80 km G.652 SMF having 16.5 dB attenuation each.

4. 1.52 Tb/s transmission experiments

Single carrier transmission experiments have been performed using a family of probabilistically constellation shaping (PCS) formats of variable entropy (H), first in B2B and after transmission through a single mode fiber (cf. Fig. 6). At H=4 bits/symbol the measured GMI is close to the theoretical value, i.e. the entropy H of the transmitted constellation. For constellation entropies <5 bits/symbol, the GMI increases proportionally to H. Beyond 5 bit per symbol the limited SNR of the transponder starts causing a deviation from this theoretical linear relation between H and GMI (dashed line). The maximum GMI of 6.2 bit/symbol is achieved at H=7.5 bits/symbol. One can explain this large difference between the required H to maximize the GMI (capacity) through the capacity versus SNR relation from the Shannon–Hartley theorem: as the transceiver has a finite SNR, one need to employ constellations of higher H to increase the capacity at that SNR, thus increasing the gap between H and the resulting GMI. As a real FEC decoding is applied for error-free recovery of the signal, the net rates are slightly lower than the GMI. The decoding loss depends on the format, varying between 0.2 to 0.45 bits/symbol. The maximum achieved error-free transmission rate (net rate × symbol rate × 2 polarizations) is 1.55 Tb/s. In a further experiment we measured the required OSNR in B2B for varying net transmission rates (cf. Fig. 7). At 800 Gb/s using dual-pol.–64QAM at H=4 bits/symbol, which could be a candidate for future 800 Gigabit Ethernet, 20.3 dB of OSNR is required with very low implementation penalty. The penalty in required OSNR increases slowly up to 1.2 Tb/s where it reaches 27.2 dB req. OSNR. Going to 1.4 and 1.5 Tb/s, is when the implementation penalty starts substantially increasing. Nevertheless, at 1.5 Tb/s the required OSNR of 36 dB is achievable at an optimum launch power of 5.3 dBm (cf. Fig. 5e). Transmission experiments over SMF are performed using PCS formats with entropy ranging from 6.5 to 7.7 bits/symbol, from which we concluded that the maximum net bitrate is achieved with H=7.5 bits/symbol. At zero spans we measured a net information rate of 6.08 bits/symbol at H=7.5 bits/symbol which reduces to 5.7 bits/symbol after 3 span transmission (cf. Fig. 8). The small drop in GMI by 0.38 bits/symbol is because the signal's SNR is still limited by the transponder's SNR rather than by optical noise. The corresponding net bitrates are 1.55 Tb/s in B2B and 1.46 Tb/s after 240 km.

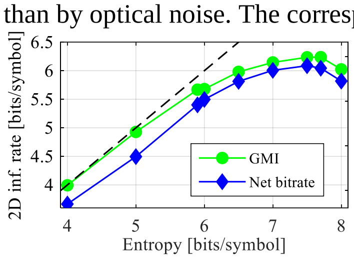

Fig. 6. GMI and net rate / bitrate versus formats entropy at 36 dB OSNR.

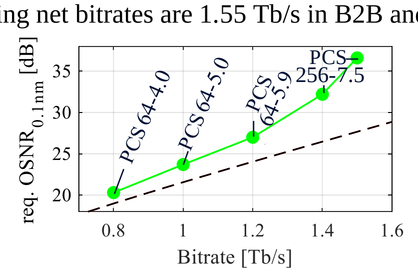

Fig. 7. Required OSNR for successful B2B transmission vs. targeted net bitrate.

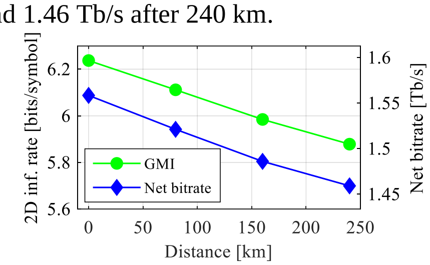

Fig. 8. Information rate and net bitrate versus SMF transmission distance.

5. Conclusions

We reported a new 128 GSa/s SiGe DAC allowing for the generation of 128 GBaud signals at information rates beyond 6.0 bits/symbol/polarization. In a single-carrier feasibility experiment we demonstrated 1.55 Tb/s in B2B, 1.52 Tb/s after 80 km, and 1.46 Tb/s after 240 km. To the best of our knowledge this is the highest single carrier bitrate rate and the highest symbol rate for systems employing a single DACs per modulated dimension reported so far.

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