Low-Cost TI-ADC Timing Calibration Circuit

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Abstract: An efficient timing skew calibration of time-interleaved ADC (TI-ADC) for high-speed link is proposed and experimentally validated. The method is based on the CDR's existing sub-blocks, and enables flexible tradeoff of complexity versus performance.
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1. Introduction

DSP-based architecture becomes preferred in high-speed links [1]. The first and most important component in the digital domain is the analog-to-digital converter (ADC). To reduce the analog design requirements and improve the ADC performance, time interleaving (TI) technique is a common approach [2]. TI-ADC includes several slower and *identical* sub-ADCs with *equal* delay between each neighbor sub-ADCs. On the other hand, due to production variations, the sub-ADCs are not identical and do not have equal delay, which lead to TI-ADC mismatches such as offset, gain and timing mismatches [3]. While offset and gain mismatches are relatively easy to calibrate, the timing skew is more challenging as its required precision is derived by the full rate time scale [3]. In most cases, the timing mismatch is detected in the digital domain and fixed in the analog domain [2]. The digital detection circuits can be based on auto-correlation, time derivation, etc. [4]. However, these methods require some assumption [4], and require additional expensive circuits. For data center inter- and intra- connection (DCI) applications, a low-cost and low-power solution is required. Thus, calibration process based on existing circuits is preferred. It this work we propose a new TI-ADC timing mismatch calibration scheme based on the existing sub-components of the clock and data recovery (CDR) circuit. The new method is robust for different phase error detectors, is shown to be immune to noise, and enables flexible design under the tradeoffs of complexity, accuracy and convergence rate.

2. Theory – CDR-based timing calibration

2.1. Timing mismatch effect

Time interleaving architecture is the common approach for high-speed and high-resolution ADCs. However, the sub-ADCs of the TI-ADC may not sample at the desired phase, which leads to constant deterministic jitter. In most practical systems, in addition to the timing mismatch related noise, other phase noises exists such as periodic (deterministic) jitter and frequency drift due to the Tx-Rx frequencies mismatch. These noises are ADC-independent, and shared between all the sub-ADCs of the TI-ADC. To overcome these shared jitter and frequency drift, CDR circuit is used. The common approach is to perform the estimation of the phase noise and phase drift in the digital domain, and overcome it in the analog domain by changing the ADC sampling phase (usually via phase interpolators (PI) which are located between the source clock and the ADC).The digital estimation part includes time error detector (TED), low-pass filter (LPF) loop (in most practical systems a 2nd order loop is used to cope with the frequency drift) and numerical control oscillator (NCO). The TED detects the difference between the real sampling phase and the desired one, and the loop averages the instantaneous errors and detects the frequency and the phase error. In most TI-ADC based system, the loop averages the errors which result from *all* the sub-ADCs, thus, it averages the timing mismatch. Therefore, even though the *average* sampling phase will be in the desired position, each sub-ADC may sample earlier or later. This loop's averaging feature mixes all the timing mismatches and essentially "hides" them.

2.2. Proposed method

In most high-speed links, due to the fact that the digital clock is slower than the symbols rate, the digital calculation should be implemented in parallel. In addition, it is common practice that the number of the digital parallel lanes is integer multiplication of the number of sub-ADCs. Thus, each digital lanes can be associated with a specific sub-ADC. Using this insight, the TED output of specific digital lane can be associated with a specific sub-ADC and can be used for its timing skew identification. The straightforward but wasteful solution is to implement a CDR and PI per sub-ADC, which get the appropriate timing per digital lane. However, this approach is too expensive due to the requirement of a 2nd order loop and PI per sub-ADC. In addition, the PI's dynamic range is a whole unit interval (UI) while in most TI-ADCs, the timing mismatch is less then UI [5] and requires less dynamic range for calibration.
Our proposed method offers to split between the "shared" and the "unique" error phases. The periodic jitter and the frequency drift are shared to all TI-ADC sub-ADCs and lead to the same timing effect on all the sub-ADCs outputs.

On the other hand, the timing mismatch is a unique phenomenon of each sub-ADC. Thus, a single 2nd order loop and a single PI are necessary only to the share effects, while the unique phase mismatch effect requires only a 1st order loop (to cope with phase noise) and an analog calibration circuit with lower dynamic range. This approach is presented in Fig. 1(a). In the proposed circuit, the TED detects in parallel all the errors of all the digital lanes but doesn't mix them. The shared 2nd order loop gets all errors, averages them and detects the shared effects. In parallel, each error is fed into a 1st order loop which detects the unique skew of the appropriate sub-ADC. Due to the fact that the timing mismatches changes very slowly, the calibration loops may work at very slow rate as compared to the shared loop.
The proposed method is hardware resources cost effective. The TED can be used as a shared circuit for both, the shared and unique errors detection. In addition, the conversion estimation from the error units (Volt) to the phase correction units (Time) for the NCO is shared for both processes. Another advantages is the complexity scaling versus the number of sub-ADCs. In the offered approach, each sub-ADC is calibrated independently, thus the system complexity increase only linearly with the number of the sub-ADCs. This is contrast to the conventional TI-ADC where the calibration is perform "at once", thus the scalability is much more challenging. As explained above, the timing mismatch is a phase phenomenon and requires only 1st order loop. However, to improve the convergence rate a 2nd order loop can be used with the cost of hardware complexity. Namely, this method allows tradeoff between convergence rate, estimation accuracy and circuit complexity.
It should be notes, that this method has not any assumptions about the TED type. Thus, it should work for any TED type, such as Mueller-Muller (M&M), Early-Late, Gardner, etc. Yet, the affiliation of all three: digital lane – timing skew – sub-ADC assumes that the TED doesn't mix between several timing skews of several sub-ADCs. This requirement may affect the TED implementation. For example, the common M&M-based TED searches for the difference between the post-cursor and pre-cursor, as is presented in the left hand side equality of Eq. (1). However, this common formula mixes between two different ADC outputs from two different sub-ADCs and hence mixes between two different timing skew. Thus, the M&M is proposed to be modified using the right hand side equality of Eq. (1) which gives similar detection signal without any timing mismatches mixing:

$$err = E[x_{n+1}y_n - x_n y_{n+1}] = E[x_n y_{n-1} - x_n y_{n+1}] \quad (1)$$

where x is the ADC output, y is the detected symbols (at the decision-device output), err is the estimated phase error and $E[\cdot]$ is the expectation operator.

3. Experimental Results and Discussion

3.1 Experimental Setup

The experiments performed were based on an end-to-end IM-DD setup. The Tx included Keysight A9125 AWG, which was followed by a bias-tee which drove a commercial VCSEL. The VCSEL was drove by 7.5 mA bias which led to a 10 GHz VCSEL BW. The data signal swing was set to 10 mA, which led to 1-3.2 mW output optical power. The data signal included PRBS13Q PAM-4 signal at 26 Gbaud. The optical channel included 100 meter MMF OM4. The receiver consisted of a Tektronix DSA8300 sampling scope with 16-bits resolution and 50 GHz analog bandwidth which sampled 100 samples per symbol (SPS). The Rx-DSP path included CDR which controlled the sampling phase and 6 taps UI-spaced FFE for signal equalization. The generator and the sampling scope were synchronized to control the jitter and frequency drift effects. The frequency drift was set to 200 parts per million (PPM) and the sinusoidal jitter was set on the 4 MHz and 0.025 UI amplitude, which is the maximum allowed value by IEEE 802.3ck and OIF CEI-56G-PAM4 standards for long-reach (LR) links. The CDR's TED was implemented as M&M and the 2nd order loop was set on 8 MHz and 0.7 dumping factor. The digital domain operated at 1 SPS and 20 parallel digital lanes. The TI-ADC was modeled by 10 sub-ADCs, so each digital parallel digital lane was associated to specific sub-ADC. The timing mismatch was modeled as zero-mean uniform distribution of 20% UI.

3.2 Calibration process

The calibration process was based on the proposed method. The calibration circuit included 10 1st order loops which were implemented by simple averaging circuit and 10 slow NCOs. To avoiding different timing mismatches mixing, the modified M&M was used, as explained in 2.2. The total calibration circuit cost (power and area) was negligible compared to the CDR circuit itself (less than 3% addition). **Fig. 1(b)** presents the convergence of the sub-ADCs timing skew versus the number of symbols which were used (in term of average error and the signal SNR). It is clearly observed that the calibration process corrected successfully the mismatches: the average error decrease to zero and the SNR converge to the SNR bound when no timing mismatch exist. The effect of mismatched mixing between different sub-ADCs in the TED signal is also depicted in Fig. 1(b) by the dashed lines. The convergence process when

the common M&M is used is compared with the modified M&N where the mismatched mixing are avoided. The results reveal that the mixing reduced significantly both the convergence rate and the steady state performance values (after the calibration process). The modified M&M clearly outperforms the classical M&M TED.

3.3 Robustness measurements

Thermal noise (as additive white Gaussian noise (AWGN)) is one of the limiting factors in DCI applications. Even though the noise decreases the TED accuracy, the loop filter reduces the variance of the estimation's error, i.e. more samples leads to more accurate estimation on the cost of longer estimation time. Therefore, by using loops with longer averaging length, the proposed method is shown to be only slightly sensitive to AWGN. **Fig. 1(c)** presents the calibration process versus different E_b/N_0values. Stronger noise leads to longer convergence period, but the steady state performance is equal to the ideal (noiseless) calibration presented by the dashed lines in the figure. As explained above the proposed method is TED methodology independent. **Fig. 1(d)** presents the SNR versus calibration iteration for M&M, Early-Late and Gardner TED (under the assumption of no mismatches mixing). It is shown that all the methodologies yield the same performance at the steady state, and with very similar convergence rates. Thus, the method is insensitive to the CDR error detection scheme itself, and can use the existing components of the CDR.

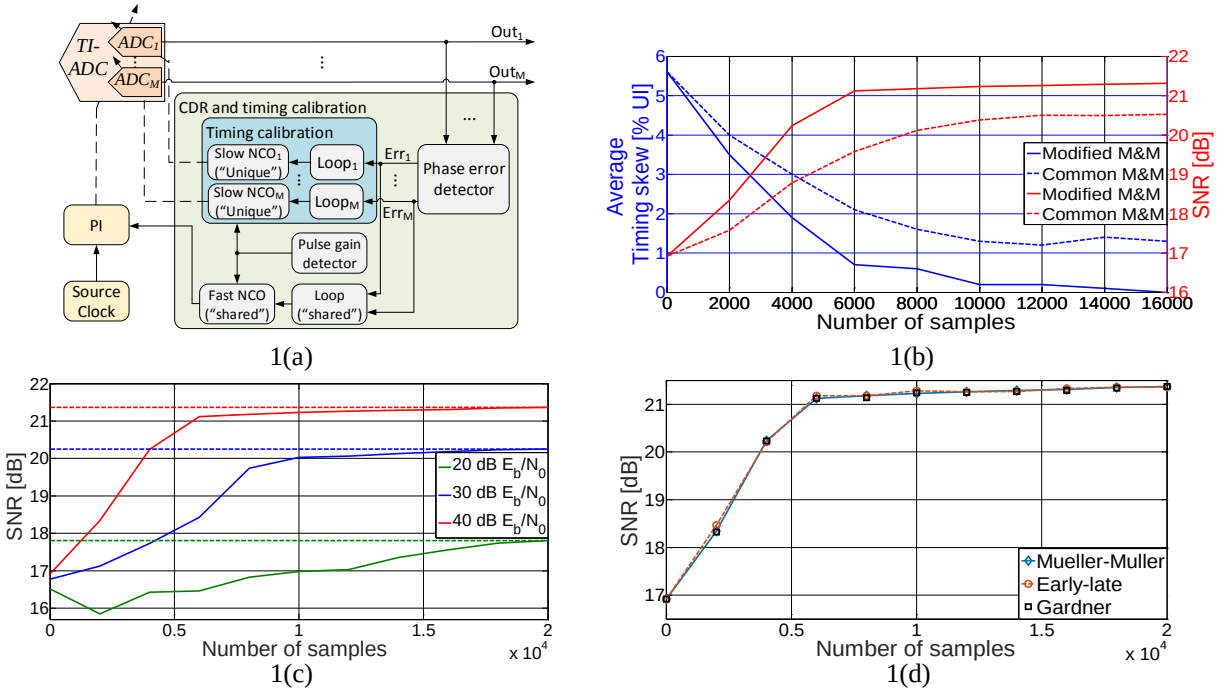

Figure 1: (a) Proposed method blocks scheme. (b) SNR convergence and average error for modified/common M&M formula. (c) Noise insensitivity. (d) TED-type insensitivity.

4. Conclusion

In this paper, a low-cost timing calibration for TI-ADC is proposed. Based on existing components of the CDR, the timing mismatch of each sub-ADC can be identified for correction in the analog domain. The proposed method is immune to noise and insensitive to TED type. A laboratory proof-of-concept of a VCSEL based 53Gbit/sec PAM4 transmission system over 100m of OM4 MMF was demonstrated, indicating the successful TI-ADC calibration, and the immunity to AWGN and TED algorithm type.

5. References

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