Optoelectronic Glass Substrates for Co-packaging of Optics and ASICs

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Abstract: A glass packaging substrate with integrated waveguides and evanescent couplers for silicon photonic chiplets is introduced for fiber to chip interconnects with high-channel counts required for co-packaging of optics and switch ASICs in next-generation datacenters. © 2020

1. Introduction

The capacity of switch Application Specific Integrated Circuits (ASICs) in datacenters has experienced exponential growth over time, having doubled every two years in the last decade. The current switch generation has a bandwidth of 12.8 Tb/s and 128 ports 100 Gb/s or 32 ports 400 Gb/s. The switch ASIC module is typically assembled on a printed circuit board (PCB) inside a single rack unit form-factor. The electrical high-speed signals are routed to the pluggable optical transceivers located at the front-panel, many centimeters away. The limiting factors for next generation switches are the required power to drive the electrical signals across a PCB and the front panel density for the optical modules [1]. Reducing the length of the electrical lines by replacing the optical modules at the front panel with optical connectors and integrating the transceiver components to the switch package will decrease the electrical path length to millimeters in length. Currently, the work on such complex multi-chip modules (MCM) is in the development stage [2]. In addition to the challenge of interconnecting the optical transceiver I/Os with optical fibers, additional packaging challenges are the co-design of signal and power distribution, thermal management, and mechanical support. For co-packaging, the switch ASIC located in the center of the module will be surrounded by the transceivers which are connected to an array of optical fibers. One scenario for a next generation 51.2 Tb/s switch ASIC is the assembly of sixteen 3.2 Tb/s photonic integrated circuits (PICs), each with sixteen fibers (eight 400 Gb/s transmitter and eight 400 Gb/s receiver channels) resulting in 256 optical fibers going to the front panel. Today, optical modules are electrically assembled first, followed by active optical alignment of a fiber array unit (FAU) or passive placement of a fiber array in precisely etched V-grooves [3] which is bonded using a UV-curing adhesive. Alternatively, initial work has been done on solder-reflow compatible fiber-to-chip interconnects to change the order of the process sequence for photonic ball grid array (BGA) package to PCB assembly [4]. High-density integrated (HDI) organic laminates for MCMs were demonstrated with dimensions of 90 mm x 90 mm [5]. A similar size would be required for co-packaging.

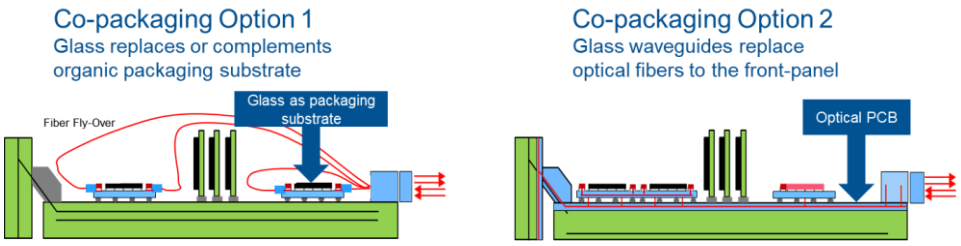

Fig. 1. Glass as a (left) packaging substrate and (right) waveguide layer for optical PCB

This work explores an optoelectronic glass substrate with optical interconnects, electrical redistribution layers (RDLs), and through glass vias (TGVs) that can enable the high-throughput pick-and-place assembly of electrical and photonic ICs as shown in Figure 1 (left). In this way, the assembly of all components is achieved by pick-and-place. The optical and electrical interface interconnection for each transceiver occur in a single assembly step. The optical interface consists of an evanescent coupler between the silicon photonics chiplet and the glass waveguides integrated in the substrate. The glass waveguides are interconnected to optical fibers via an optical fiber array connector. The length of the glass waveguides could be extended all the way to the front-panel to replace fiber fly-overs shown as Option 2 in Figure 1.

2. Glass Waveguides

Thermal ion-exchange is a batch process where multiple glass sheets can be processed in parallel for scalability and lowest cost. An ion-exchange process resulted in buried waveguides, where the waveguide core center position is located a few microns underneath the glass surface. Corning Laser Technologies' novel ultrafast laser nano-perforation process was employed to cut the glass substrate and leave optical quality end-faces around the ion-exchanged waveguides. This enabled low-loss optical edge coupling with no additional post-processing steps to smooth the surface (e.g., polishing) after separation while a mechanical force or in some cases exposure to CO_2 laser irradiation was applied to the perforation line as shown in the cross-section of Figure 2 for separation.

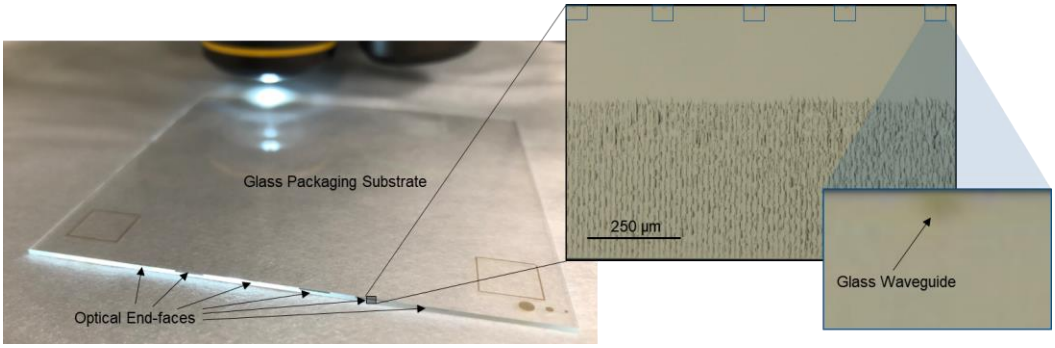

Fig. 2. Glass packaging substrate (70 mm x 70 mm) and cross-section view of laser-cut optical end-face

Waveguide propagation loss was measured to be 0.08 dB/cm at 1310 nm wavelength using the cut-back method with single-mode fiber launch and detection and index-matched interfaces. Waveguides with a refractive index increase of 0.005 closely matched the fiber mode and resulted in 0.3 dB coupling loss per end-face. As a result of the low index contrast, the bend loss increased exponentially for bend radii smaller than 30 mm. In contrast, a different waveguide design had a refractive index increase of 0.009 which resulted in lower bend losses and a smaller minimum bend radius of 10 mm. Simulations revealed < -60 dB cross-talk for two parallel waveguides of 3 mm in length with 50 µm pitch. Figure 2 shows a glass substrate (70mm x 70mm) with all four edges along accessible for fiber connectivity, and the optical routing in the glass substrate enables efficient pitch conversion between the fiber array interface (e.g. 250 µm) and the optical ports of the PIC (e.g. 50 µm) inside the substrate.

3. Evanescent PIC Coupler

Integrated glass waveguides are localized just below the surface of the glass substrate, which enables implementation of an optical interface to a PIC waveguide based on evanescent mode coupling, without additional processing of the glass surface. The evanescent coupler has certain advantages, such as vertical integration, wide bandwidth and polarization control, but imposes more stringent requirements on the tolerance to variations in the separation between the waveguides. Figure 3a shows an example cross-section of a glass waveguide mounted on top of a Si-wafer stack featuring a Si-waveguide with 450 nm x 220 nm nominal cross-section. The optically transparent adhesive between glass and Si chips provides mechanical contact and controls waveguide separation. Large difference in the refractive indices of the glass and Si-waveguide necessitate an adiabatic reduction of the Si-waveguide width from 450 nm to ~100 nm to achieve phase matching and efficient power transfer between modes of the two waveguides. Figure 3b shows the variation of the taper width along its length, computed using non-linear taper design method [6]. This approach considers mode mismatch dependence on the taper width, quantified by computing consecutive mode overlap integrals as a function of location along the taper, to optimize the taper width gradient with respect to the propagation distance, under the constraint of a low loss target. Figure 3c illustrates the optical loss at 1310 nm, computed using the Eigenmode Expansion Method, for evanescent coupling between an ion-exchange glass waveguide and a tapered Si-waveguide. Theoretically, a coupling loss of <0.5 dB can be achieved for a 1 µm thick adhesive with 2.5 mm long tapers, provided that the refractive index of the adhesive is close to the target value. Analysis of the loss dependence on the adhesive thickness indicates that taper lengths > 2 mm, or adhesive thickness < 1.5 micron are required to maintain low coupling loss. Tolerance to lateral misalignments between the waveguides is found to be 2.5-3 µm for < 0.5 dB increase in coupling loss.

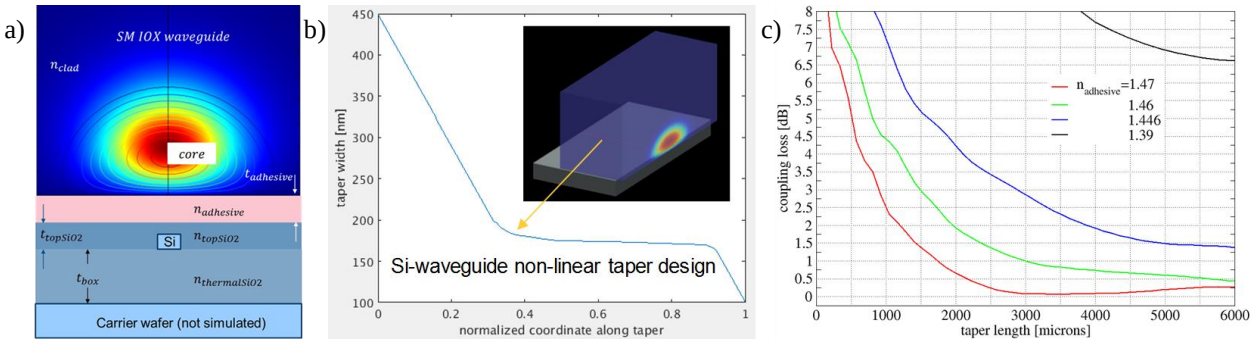

Fig. 3. a) Cross-section view of an ion-exchange (IOX) glass – Si-waveguide stack. b) Taper width design optimized for low loss, short length coupler. c) Coupling loss dependence on the taper length and adhesive refractive index, computed for $t_{adhesive}$=1 μm.

4. Glass Packaging Substrate

With serial electrical line rates for 51.2 Tb/s switches expected to increase from 56 Gb/s to 112 Gb/s per lane, heterogenous integration of switch ASICs and PIC transceivers onto a common package substrate reduces the electrical interconnect loss by decreasing reach from at least 100 mm across the PCB to the front panel to ≤ 50 mm across the substrate package. The decreased reach helps counteract the effects of the higher electrical loss at the doubled Nyquist frequency and is expected to reduce the link power budget by ~20%. However, there are significant electrical, thermal and mechanical packaging challenges particularly resulting from substrate sizes approaching 100 mm x 100 mm for co-packaging. New materials and assembly approaches are needed for: low loss and power efficient high-speed electrical interconnects; thermal management of a high-power consuming ASICs on the same substrate as temperature sensitive PICs; low substrate warpage, and high electrical reliability of chip-to-package substrate bumps/pillars and substrate-to-board ball grid array (BGA). Glass has a unique combination of properties that well-position it for these co-packaging challenges.

Our approach consists of a single glass substrate where the top redistribution lines (RDLs) connect high speed electrical lanes between the ASIC and the optical transceivers along with TGVs providing power and ground to the ASIC and optical transceivers. The single layer provides simpler fabrication and assembly compared to 2.5D silicon interposer on an organic substrate or embedded multi-die interconnect bridge configurations so has the potential for lower overall packaging cost. Glass substrates as formed by a fusion draw process inherently has exceptional surface smoothness and the necessary flatness and dimensional stability for small line and space RDLs of tight geometric control, comparable to silicon and far better than organic substrates. Yet unlike silicon, it can be formed in large formats that contain a large number of package substrates for cost effective, panel-level processing. Corning Laser Technologies' process can not only singulate panels into substrates, it can create complex cutouts at the substrate edge for fiber optic connector housings and create the TGVs. Another important consideration for such large package substrates is warpage. Glass has a much higher modulus and hence stiffness than organic materials, and a coefficient of thermal expansion (CTE) that can be adjusted to that of silicon or between silicon's CTE and that of a PCB. This should provide high bump and ball interconnect assembly yields and high-power cycling reliability.

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