5.7-dB Fiber-to-Fiber Loss 8 × 8 Silicon Photonics Switch with Port-Alternated Switch-and-Select Architecture

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Abstract: We propose and demonstrate a Port-Alternated Switch-and-Select architecture that has both low insertion loss and low path dependency. Using silicon photonics platform, we realized an 8 × 8 switch with 5.7-dB Fiber-to-Fiber insertion loss. © 2020 The Author(s)

1. Introduction

Optical switches play important roles in future energy-efficient telecom and datacom networks [1,2]. Silicon photonics switches are particularly important because they provide compactness, high reliability, mass productivity and fast switching time [3]. Most of silicon photonics platforms are based on single layer in which intersections between waveguides are unavoidable, leading to larger insertion loss and crosstalk. Recently, multi-layer platforms have been reported to avoid crosstalk at the intersections [4,5]. However, it causes complexity of the process and additional insertion loss from interlayer transfer structures. In this paper, we focus on a single-layer optical circuit and propose a strictly nonblocking switch architecture which has both low loss and low path dependency even with single-layer circuits. We also demonstrate an 8 × 8 silicon photonics switch based on the architecture and demonstrate 5.7-dB fiber-to-fiber insertion loss with low crosstalk of less than −30 dB.

2. Architecture

Strictly nonblocking switch topologies on planar circuits can be classified into three: cross-point topology [6], path-independent loss (PILOSS) topology [7], and switch-and-select (SAS) topology or double-layer network [8]. Table 1 summaries the worst insertion loss, path-dependent loss and crosstalk of each topology, where double-gate configuration for crosstalk suppression is adopted and 2 × 2 Mach-Zehnder Interferometers (MZI) are used for the element switches. Here, L_{MZ} and L_{IS} denote the insertion losses of a single element switch and an intersection, respectively, and X_{IS} denotes the crosstalk value of an intersection. As shown in Table 1, the worst insertion loss is much small in SAS topology as compared to Cross-point and PILOSS topology. However, PILOSS topology has zero path-dependent loss which is preferable when used in actual systems, where SAS topology has relatively large path dependent loss when N is large. Thanks to the double-gate configuration, the crosstalk amount is the same among the three topologies. Realizing both small insertion loss and small path dependency is of crucial importance in designing large port count switches. Here, we propose a new architecture, Port-Alternated Switch-and-Select (PA-SAS) architecture which has both low insertion loss and low path dependency as also shown in Table 1. The construction method of this architecture is described below.

Table 1. Comparison of Strictly Nonblocking Switch Topology

	Cross-point	PILOSS	SAS	PA-SAS (proposed)
Worst insertion loss	$(N + 1)\,L_{MZ}$ + $O(N^2) \times L_{IS}$	$(N + 1)\,L_{MZ}$	$(2\log_2 N)\,L_{MZ}$ + $O(3N) \times L_{IS}$	$(2\log_2 N)\,L_{MZ}$ + $O[(11/6)\,N] \times L_{IS}$
Path-dependent loss	$N\,(N - 1)\,L_{IS}$	0	$O(3N) \times L_{IS}$	$O[(2/3)\,N] \times L_{IS}$
Crosstalk	$(N - 1)\,X_{IS}$	$(N - 1)\,X_{IS}$	$(N - 1)\,X_{IS}$	$(N - 2)\,X_{IS}$

Figure 1 (a) shows a schematic illustration of 2 × 2 switch as a building block of the architecture. Here, the black 1, 2 ports indicate input ports and the red 1', 2' ports indicate output ports, which are placed in major and minor diagonal positions, respectively. The black circles denote 1 × 2 element switches, which can be realized by MZIs as shown in Fig. 1 (b). Fig. 1 (c) shows a schematic illustration to construct a general $N \times N$ switch, where N is power of 2. The $N \times N$ switch can be constructed from $(N/2) \times (N/2)$ switch recursively. The input/output ports are placed at major/minor diagonal positions in four quadrants, and are connected to four $(N / 2) \times (N / 2)$ switches. The resulted optical switch has the same connections between the element switches as the SAS topology. However,

thanks to the port-alternated configuration, the number of intersections between waveguides are significantly reduced. As shown in Table I, conventional SAS topology has maximally O(3*N*) intersections and minimally no intersections. On the other hand, PA-SAS architecture has maximally O[(11/6) *N*] intersections and minimally O[(7/6) *N*] intersections. Therefore, both the maximal insertion loss and path-dependent loss can be suppressed using the proposed architecture.

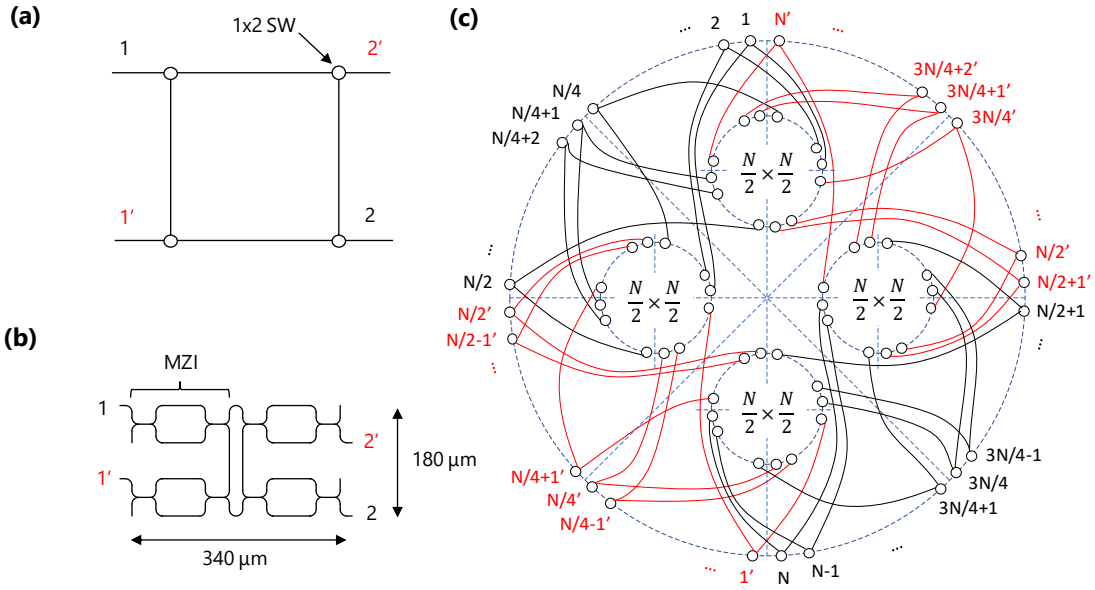

Fig. 1. (a), (b) Schematic illustration of the 2 × 2 switch. (c) Construction scheme of PA-SAS architecture corresponding to a *N* × *N* switch, where *N* is power of 2.

Figure 2 (a) shows a numerical comparison of each architecture in the viewpoint of loss. For the calculation, MZI/intersection losses of 0.25 dB/0.028 dB are used as typical values from our fabrication results. Loss of connecting waveguides are neglected in the calculation. As shown in Fig. 2 (a), PA-SAS architecture has the lowest loss. A 2D map of Fig. 2 (b) shows that the PA-SAS architecture has both low on-chip loss and low path-dependent loss for the case of *N* = 32. Encouraged by these results, we fabricated and measured the characteristics of the 8 × 8 PA-SAS topology silicon photonics switch in the following section.

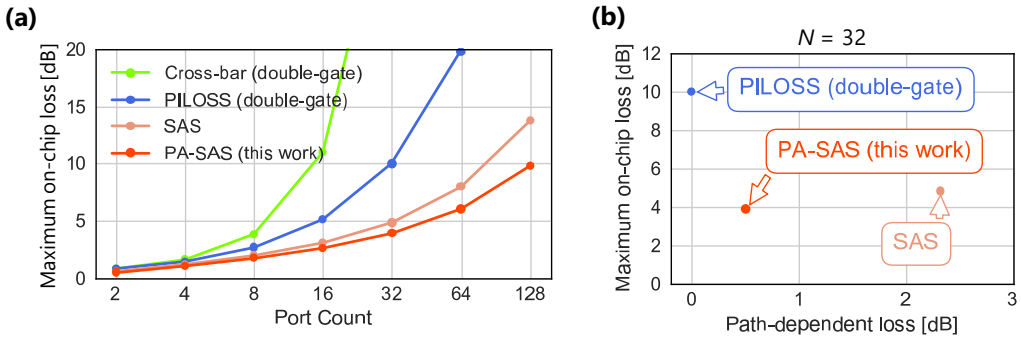

Fig. 2. (a) Numerical calculation results of maximum on-chip loss for each switch architecture. (b) A 2D map of path-dependent loss and maximum on-chip loss for the case of *N* = 32.

3. Device Fabrication and Measurement

Figure 3 (a), (b) show a schematic structure and a micrograph of a fabricated 8 × 8 silicon photonics switch based on the PA-SAS architecture, respectively. The footprint of the 8 × 8 switch part is just 3 × 3 mm^2, which is as small as

other switch architectures. The device is designed for Transverse-Electric-like (TE-like) mode, and on-chip polarizers are used as polarization cleaners. A 20-core high-Δ fiber array (fusion spliced to standard SMFs) is attached to the chip edge, where the SMF-chip coupling loss was ~1.2 dB/facet which is measured from a "pass-through" waveguide on the same chip. Fig. 3 (c) shows results of all-path transmission of the 8 × 8 switch. As shown in this figure, the leakage to the unwanted output ports are mostly suppressed by more than −40 dB. The measured fiber-to-fiber insertion loss was 5.7 ± 0.75 dB. The loss fluctuation could be originated from core position errors of the fiber array and roughness of the chip edge. Applying an additional polishing to the edge would improve the variation. The breakdown of the loss is considered as follows. The fiber-chip coupling loss was ~1.2 dB/facet. Polarization cleaners have loss of ~0.6 dB. Guiding loss from the chip edge to the switch part is about 0.8 dB (7.4 mm). Loss of the switch part is ~1.5 dB from Fig. 2 (a). The summed loss of ~5.3 dB well describes the measured value. If we see Input 2 of Fig. 3 (c), there are two points that show larger leakages than other points. This could be because several MZI element switches have imperfections in the fabrication. We consider that these leakages can be suppressed by inserting additional gate switches. We measured the crosstalk spectrum of a path that include these leaky switches, and the results are shown in Fig. 3 (d). As shown in the figure, even in this path, the crosstalk is suppressed by more than −30 dB for broad wavelength range thanks to the double-gate configuration.

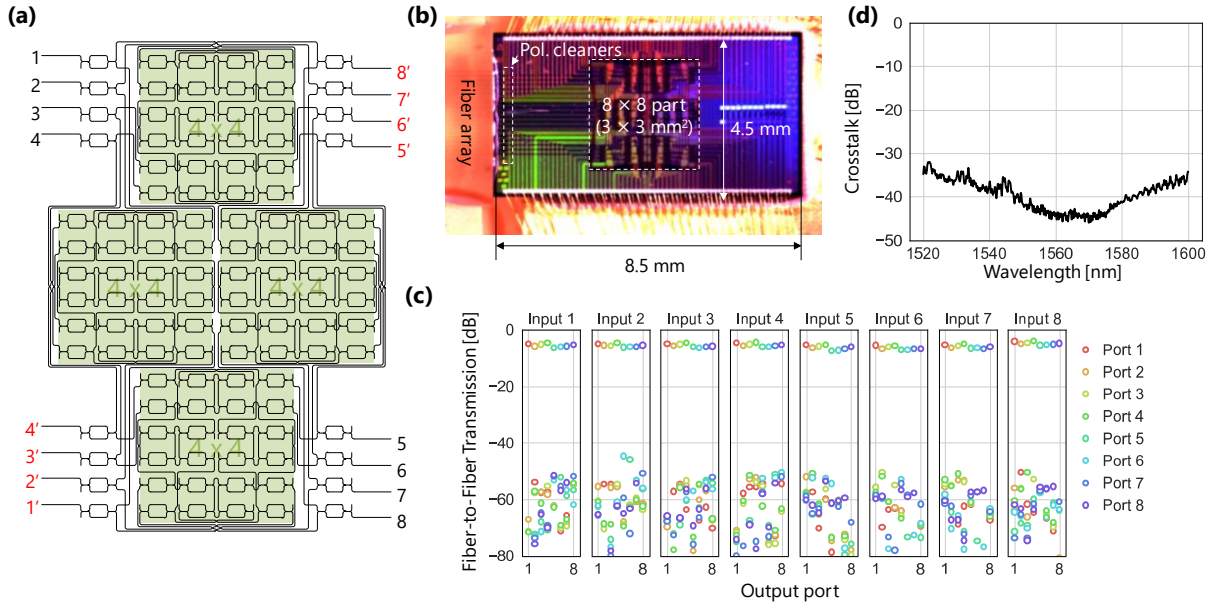

Fig. 3. (a) Schematic structure of the 8 × 8 PA-SAS switch. (b) Micrograph of a fabricated sample. (c) Measured results of all-path transmission. (d) Measured crosstalk spectrum of the path that include the largest leakage measured in all-path transmission measurement.

4. Conclusion

In this paper, we have proposed a novel switch architecture, PA-SAS, and demonstrated a 5.7-dB fiber-to-fiber loss 8 × 8 switch. The next target would be realization of larger port count switches such as 32 × 32.

5. References

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