Large-area Metalens Directly Patterned on a 12-inch Glass Wafer using Immersion Lithography for Mass Production

Qize Zhong[*†], Yuan Dong[†], Dongdong Li, Nanxi Li, Ting Hu, Zhengji Xu, Yanyan Zhou, Keng Heng Lai, Yuan Hsing Fu, Vladimir Bliznetsov, Hou-Jang Lee, Wei Loong Loh, Shiyang Zhu, Qunying Lin, and Navab Singh

Institute of Microelectronics, Agency for Science Technology and Research, 2 Fusionopolis Way, #08-02, Innovis, Singapore 138634
[†]These authors contributed equally to this work, [*]Email: zhong_qize@ime.a-star.edu.sg

Abstract: We developed a technology to directly process 12-inch glass wafers using 193 nm immersion lithography for metasurface devices fabrication. An 8-mm-dimeter metalens working at 940 nm wavelength has been demonstrated as a proof-of-concept functional device.

OCIS codes: (220.0220) Optical design and fabrication; (110.5220) Photolithography; (310.6628) Subwavelength structures, nanostructures.

1. Introduction

Flat optics devices are based on engineering the spatial distribution of optical phase on a two-dimensional (2-D) surface through a subwavelength-thick metasurface layer. This revolutionary technology enables novel metasurface-based optical elements such as lens, waveplates, deflectors, and filters, *etc*.[1] So far, most of the metasurface devices operating at visible and near-infrared wavelengths were fabricated on glass or quartz substrates using electron beam lithography (EBL) [2], which is not suitable for mass production because it requires hours of writing time. In order to push the metasurface technology from lab to fab, it is highly demanded to fabricate metasurface devices using the mature silicon complementary metal-oxide semiconductor (CMOS) fabrication technology [3]. The deep ultra-violet (DUV) photolithography used in the standard CMOS manufacturing line, *e.g.* the 193 nm immersion lithography, meets the requirement of patterning the small feature size of metasurface devices [4,5]. However, it is challenging to handle the transparent glass or quartz wafers in the CMOS processing tools because all these tools are designed for silicon wafers. To circumvent this difficulty, a "layer transfer" technology was developed, in which the metasurface layer was first fabricated on a 12-inch silicon wafer and then "transferred" to a glass wafer by a special wafer bonding and de-bonding process [6,7]. A more intuitive way is to directly fabricate nanostructures on the 12-inch glass wafers using CMOS facilities. Although progress has been made on realizing metasurfaces on small size wafers [3], the direct processing of 12-inch glass wafers using advanced CMOS infrastructures has not been reported yet.

In this work, we report the first demonstration of an 8-mm-diameter a-Si metalens which is directly patterned and etched on a 12-inch glass wafer. A technology to directly process 12-inch glass wafers in the CMOS processing tools is developed. The developed process platform is also feasible for other dielectric materials for metasurfaces, *e.g.* TiO_2 and Si_3N_4, which paves a way for the mass production of low-cost and high-performance metasurface devices in both visible and infrared wavelengths.

2. Glass Wafer Process

Fig. 1(a) shows the schematics of process flow. The starting is a 12-inch fused silica glass wafer on which a backside opaque layer is deposited. This backside opaque layer is necessary for the following dry etch processes. First a 400-nm a-Si film for metasurface elements was deposited using a plasma-enhanced chemical vapor deposition (PECVD) tool. The tool can handle glass wafers by manually loading and turning off the sensor. Then, an ultrathin opaque layer was deposited via physical vapor deposition (PVD). This layer is to make the lithography focus on the front surface. After deposition, the glass wafer is no longer transparent in the visible wavelength range. Another requirement is that the wafer warpage must be small enough for the subsequent lithography and dry etch processes. The wafer was then patterned using the 193 nm immersion lithography, followed by dry etch of the top opaque layer and the 400-nm thick a-Si layer. After photoresist stripping, the front and backside opaque layers were removed without attacking the patterned a-Si nanostructures and the glass substrate. Fig. 1(b) shows the photograph of the fabricated 12-inch glass wafer. It contains 61 full dies with dimension of 26 mm×33 mm (*i.e.*, the reticle size), as shown in Fig. 1(c). Each die contains various metasurface devices, which will be reported elsewhere. Here, we focus on the 8-mm-dimeter metalens as a proof-of-concept device.

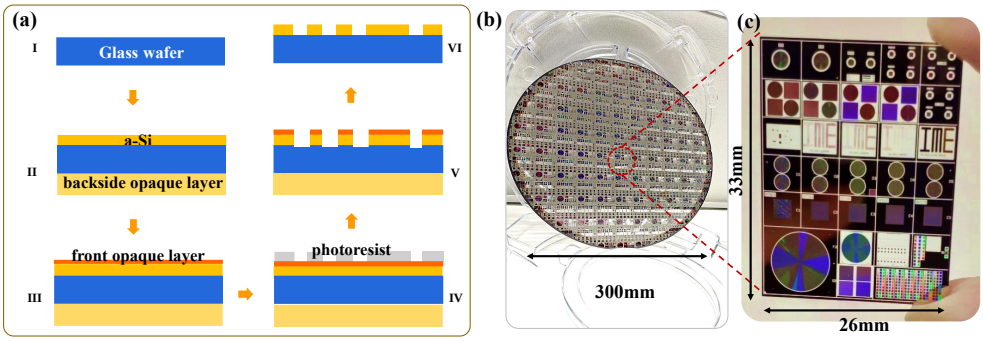

Figure 1. (a) Schematic of process flow for directly processing 12-inch glass wafer: (I) 12-inch bare glass wafer. (II) A 400-nm a-Si layer and two opaque layers were successively deposited on the front and backside of the wafer. (III) An ultrathin opaque layer was subsequently deposited to the front side. (IV) The prepared wafer was patterned using 193 nm immersion lithography, followed by ICP etching of the metasurface layer (V); (VI) the front and backside opaque layers were removed without attacking the a-Si nanostructures and the glass substrate. (b) The photograph of the fabricated 12-inch glass wafer. (c) The photograph of one die containing various metasurface devices, including an 8-mm-dimeter metalens at the lower left corner.

3. Large-area Metalens Design and Characterization

The schematic of the designed large-area metalens is shown in Fig. 2(a) to present the concept of focusing function. The metalens is formed by the unit cell containing a-Si nanopillar with fixed height of 400 nm on glass substrate. The perspective view and the side view of the unit cell are shown in Figs. 2(b) and 2(c) respectively. The size of the unit cell is 400 by 400 nm. The phase shift of each unit cell is calculated using finite difference time domain method (Lumerical FDTD^{TM}). The phase shift profile with respect to nanopillar diameter and wavelength is plotted in Fig. 2(d), which is used to form the metalens layout. The dashed line indicates the working wavelength of 940nm. A predicated focusing performance of the metalens is also simulated by using FDTD with lens diameter of 20 μm. The power intensity distribution along the propagation direction is shown in Fig. 2(e) with the inset showing the cross section at the focusing spot, from which, the spot size, *i.e* full width at half maximum (FWHM) of the spot profile, is read to be ~1.1 μm and the focusing efficiency is calculated to be 55.4%. The focusing efficiency here is defined as the ratio of the optical power in the focal spot center with a square area of $(4\times FWHM)^2$ to the incident power.

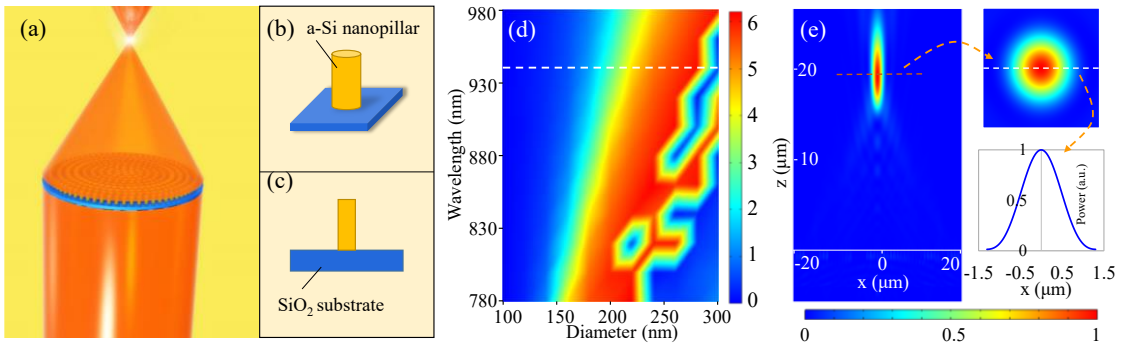

Figure 2. (a) Schematic of metalens presenting the concept of focusing function (drawing not to scale). (b) The perspective view, and (c) side view of a-Si nanopillar on the glass substrate in one unit cell. (d) The phase calculated by Lumerical FDTD in one unit cell, which is a function of the incident wavelength and nanopillar diameter. (e) The simulated power intensity distribution along the propagation direction (left) and at the focal plane (right top). The curve (right bottom) is the power intensity profile along the while dash line at the focal spot plane.

The photograph of the 8-mm-diameter metalens is shown in Fig. 3(a). The scanning electron microscopy (SEM) images of the metalens surface after opaque layer removing is shown in Fig. 3(b). The zoomed-in top view of the central location and the tilted view of the edge are included in Figs. 3(c) and (d) respectively. The tilted angle of the image is 45°. From the SEM inspections, it is found that small pillars in some locations are missing, especially at the metalens edge area, which may be attributed to the removing process for top opaque layer. Moreover, from cross-sectional transmission electron microscopy (XTEM) inspection as shown in Fig.3 (e), we notice the profile of the a-Si pillar is not perfect, e.g. the critical dimension (CD) of the a-Si pillars has a relatively large deviation from the simulated structure.

To characterize the focusing performance of the metalens, a home-made chip-level measurement system was setup, as described in [8]. The incident beam with a dimeter of 8 mm was illuminated on the metalens. The power intensity distribution along the propagation direction after the lens is measured and plotted out in Fig. 3(f), showing that the metalens has good focusing function. Fig.3 (g) shows the intensity distribution at the focal plane, where the spot size (FWHM) of ~1.5 μm is recorded. The transmission is measured to be ~57% and numerical aperture is 0.45. Whereas if the incident beam dimeter was reduced to 3 mm and being illuminated on the center of the metalens, the transmission is measured to be ~83%, indicating that the metalens edge may contains more process-induced imperfections. Here we present a proof-of-concept demonstration, and the process optimization is ongoing to further improve the metalens performance.

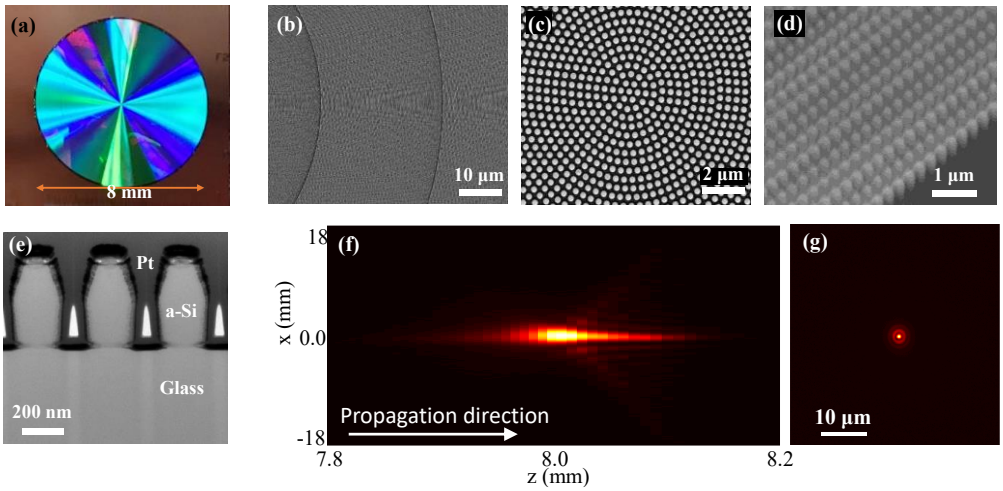

Figure 3. (a) The photograph of the fabricated 8-mm-diameter metalens (b) The SEM of the 8 mm metalens surface after removing the opaque layers. Zoomed-in top view of the central location (c) and tilted view of the edge (d) of the 8 mm metalens. The tilted angle in (d) is 45º. (e) The TEM of nanopillars, Pt here is for TEM sample preparation. The experimental power intensity distribution along the propagation (f) and at the focal plane (g), indicating the focusing effect.

4. Conclusion

In summary, a technology is developed to directly process 12-inch glass wafers in the state-of-the-art 193 nm immersion lithography based silicon CMOS manufacturing lines. A large-size metalens with diameter of 8 mm is designed and fabricated using the developed platform as a proof-of-concept device. It exhibits attractive performance and also potential for further performance improvement by process optimization. This work paves a way for the mass production of low-cost and high-performance metasurface devices.

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5. References

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