Low Parasitic Capacitance III-V/Si Hybrid MOS Optical Modulator toward High-speed Modulation

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Abstract: We present advanced design of III-V/Si hybrid MOS optical modulator to reduce parasitic capacitance and resistance toward high-speed modulation. We successfully achieved 21 times smaller RC constant, improving the trade-off between modulation efficiency and bandwidth.

OCIS codes: (130.3120) Integrated optics devices; (230.4110) Modulators.

1. Introduction

The wide deployment of 5G technology is expected to bring tens of billions of smart devices connected through internet, where cloud data centers will provide computing power and storage for these intelligently connected devices. To develop further high-performance and energy-efficient data centers, a high-speed Si optical modulator with low energy consumption is highly desired. On Si photonics platform, metal-oxide-semiconductor (MOS) optical modulators are attractive in terms of the balance of modulation efficiency and modulation bandwidth [1, 2]. In our previous study, we have reported a high-efficiency III-V/Si hybrid MOS optical modulator by bonding a thin n-type InGaAsP membrane on a p-type Si waveguide [3-5]. Compared with its Si counterparts, the modulation efficiency was enhanced by a factor of 5 – 8 with only one tenth optical absorption.

To realize high-speed optical modulation using a III-V/Si hybrid MOS optical modulator, the reduction in resistance-capacitance (RC) constant is critical. Figure 1(a) shows a cross-sectional schematic of a III-V/Si hybrid MOS optical modulator reported in [4]. In previous demonstrations, we used a 1-µm-wide Si rib waveguide for making it easy to integrate a III-V taper on the top of it. As a result, such a wide Si rib waveguide had significantly increased the RC constant without benefiting the modulation efficiency. Moreover, a III-V membrane had to lay on Si terraces on the both sides of the Si waveguide to achieve robust wafer bonding, leading to large parasitic capacitances between the III-V membrane and Si terraces. Since these parasitic capacitances are rather greater than an intrinsic MOS capacitance (C_{mod}) shown in Fig. 1(a), the modulation bandwidth cannot be enhanced. In addition, an electrode was directly contacted with a moderately doped n-type InGaAsP layer, making it difficult to achieve a low contact resistivity. Similarly, the doping density of Si layer was not high enough to enable a low-resistivity contact.

In this study, we have adopted a new design, as shown in Fig. 1(b), to address the problem of the large RC constant in a III-V/Si hybrid MOS optical modulator. Firstly, the width of Si rib waveguide in the phase shifter region was set to 400 nm which was same as that of the single-mode Si strip waveguide used in the passive part of a Mach-Zehnder interferometer (MZI). Secondly, we used a Si rib waveguide embedded in SiO_2 layer. The embedded SiO_2 layer provided physical support for the III-V membrane, eliminating all the parasitic capacitances. Thirdly, a heavily doped n-type InGaAs/InP layer was inserted between n-type contact and an InGaAsP layer, reducing the contact resistivity. Lastly, the doping densities of the n-InGaAsP and Si layers were optimized to achieve further reduction in the parasitic resistance, as shown in Fig. 1(b). Combining all the improvements, the RC constant was effectively reduced, leading to increasing the modulation bandwidth.

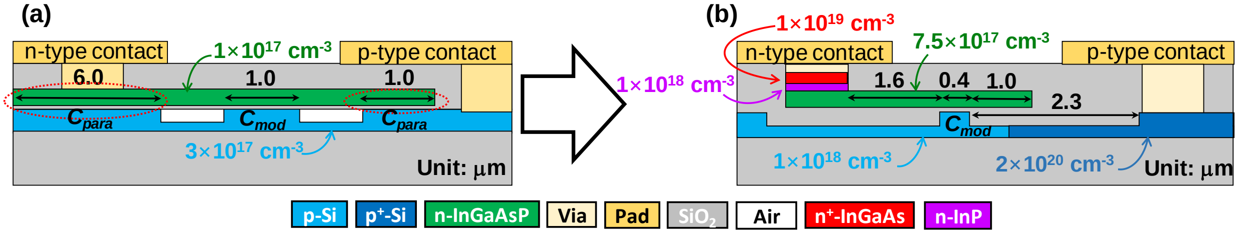

Fig. 1. Cross-sectional schematics of III-V/Si hybrid MOS optical modulators using (a) a Si rib waveguide and (b) a Si rib waveguide embedded in SiO_2 layer studied in this paper.

2. Numerical analysis

For MOS optical modulators, the modulation efficiency and modulation bandwidth are in a trade-off relationship. The modulation efficiency is proportional to a MOS capacitance, which means a larger capacitance leads to higher modulation efficiency and smaller $V_{\pi}L$. On the other hand, the cut-off frequency f_c is determined by a RC constant via $f_c = \frac{1}{2\pi RC}$. Figure 2(a) shows the dependence of modulation efficiency $V_{\pi}L$ on the width of Si rib waveguide with an equivalent oxide thicknesses (EOT) of 20 nm. For a width of 200 nm, $V_{\pi}L$ was high due to less confined optical mode. With the waveguide width increasing from 400 nm to 1000 nm, the $V_{\pi}L$ slightly decreased owning to better overlap between the optical mode and accumulated free carriers. On the other hand, with the increase of waveguide width, the modulation bandwidth dropped rapidly, as shown by the red line in Fig. 2 (b), because the capacitance scales linearly with the waveguided width. Compared with the previous design, as shown by the blue line in Fig. 2(b), the cut-off frequency was effectively enhanced by removing parasitic capacitances and optimizing doping profiles. In order to strike a well balance between modulation efficiency and modulation bandwidth, we introduced a figure of merit (FOM) defined as modulation bandwidth over $V_{\pi}L$. Figure 2(c) shows the relationship between this FOM and the width of Si waveguide. When the width was 400 nm, the FOM was maximized, indicating the optimized balance of modulation efficiency and modulation bandwidth. Hence, we adopted a 400-nm-wide Si waveguide in the following device fabrication.

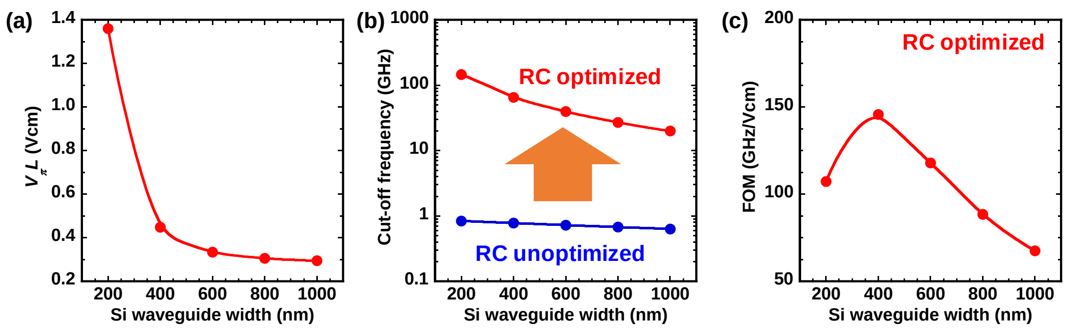

Fig. 2. (a) $V_{\pi}L$, (b) cut-off frequency, and (c) FOM versus the width of Si rib waveguide of various EOT values.

3. Fabrication and evaluation of III-V/Si hybrid MOS optical modulator

Figures 3(a) to 3(d) show the process flow of the III-V/Si hybrid MOS MZI optical modulator. After the fabrication of Si rib waveguides and boron implantation, a thick TEOS SiO_2 layer was deposited. Figure 3(a) shows a scanning electron microscope image of the Si wafer that is being planarized by chemical mechanical polishing (CMP). To reduce the SiO_2 thickness further, additional CMP was carried out as shown in Fig. 3(b). After the CMP process, the thickness of SiO_2 remaining on the Si waveguide was around 10 nm. Thanks to the planarized surface, the III-V

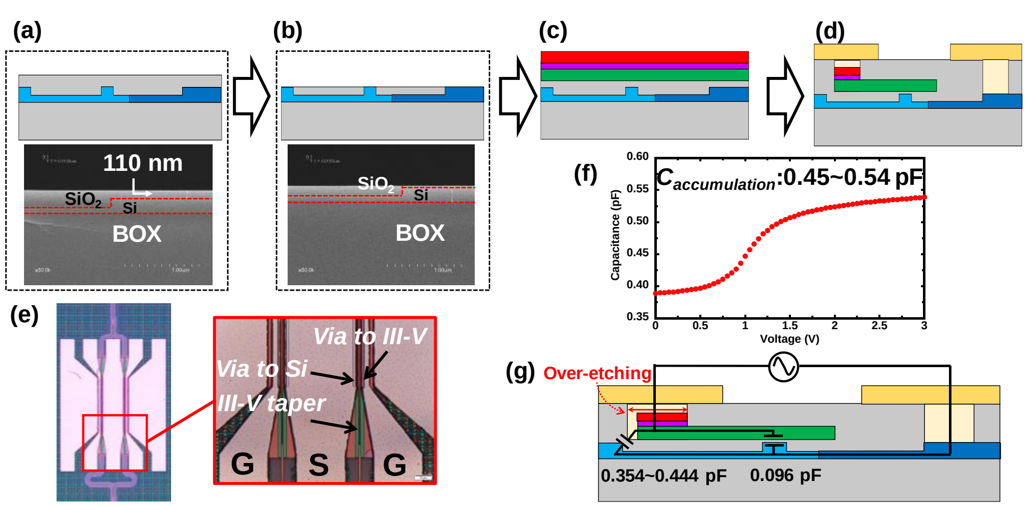

Fig. 3. (a) - (d) Fabrication process flow, (e) microscope images, (f) *C-V* curve of the fabricated III-V/Si hybrid MOS optical modulator, and (g) distribution of capacitances.

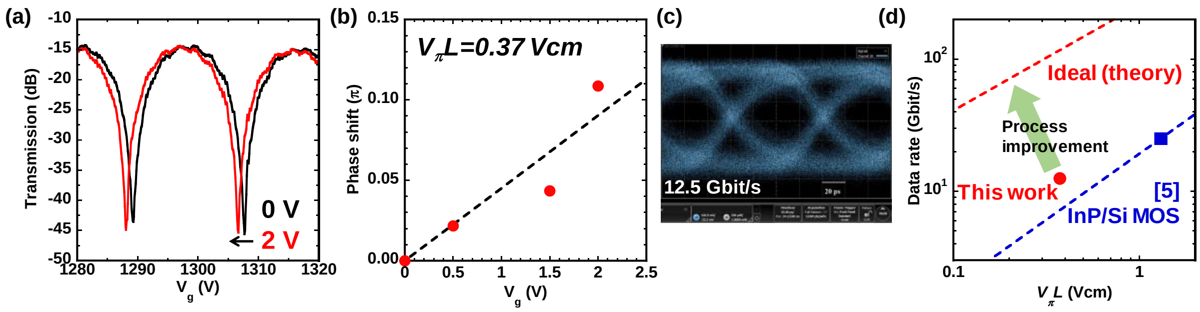

Fig. 4. (a) Transmission spectra of a fabricated MZI optical modulator, (b) measured optical phase shift as a function of gate voltage, (c) measured eye pattern at 12.5 Gbit/s, and (d) relationship between modulation efficiency and data rate.

membrane was successfully bonded on the Si waveguide after Al_2O_3 deposition on both wafers. After III-V bonding, the III-V mesa was defined by electron-beam (EB) lithography and reactive ion etching (RIE), which was followed by SiO_2 passivation and metallization. Figure 3(e) shows two microscope images of the fabricated asymmetric MZI optical modulator. Figure 3(f) shows a capacitance-voltage (C-V) curve of the 120-μm-long phase shifter. The accumulation capacitance was 0.45 pF~0.54 pF, which was 4 times smaller than that of the previous device [4], but 5~6 times larger than expected. The comparatively larger capacitance was due to the over-etching of contact via on SiO_2 cladding layer, resulting in a parasitic capacitance between the III-V membrane and Si slab as shown in Fig. 3(g). This parasitic capacitance can be removed by process optimization. Despite of parasitic capacitance, the RC constant of the advanced design was 21 times smaller than that of the original design reported in [4], even assuming the same EOT in both designs.

The fabricated MZI optical modulator with a 120-μm-long phase shifter was characterized in O-band with various gate voltages applied. Figure 4(a) shows the measured transmission spectra near a wavelength of 1310 nm. The phase shift as a function of gate voltage was presented in Fig. 4(b). From the gradient of the plot, $V_\pi L$ was extracted to be 0.37 Vcm, indicating an EOT of 17.2 nm. Owing to the low parasitic RC design adopted in this paper, we achieved a clear eye pattern at 12.5 Gbit/s as shown in Fig. 4(c). Figure 4(d) shows a benchmark between data rate and $V_\pi L$ among III-V/Si hybrid MOS optical modulators. Thanks to the advanced design and the InGaAsP membrane, we successfully improved the trade-off relationship between data rate and $V_\pi L$ as compared with InP/Si hybrid MOS optical modulator reported in [6]. Note that the superior InGaAsP/Al_2O_3 MOS interface might also contribute to this improvement. We expect that further improvement is attainable by removing the remaining parasitic capacitance through process improvement as indicated a red broken line in Fig. 4(d).

4. Conclusions

We have demonstrated a III-V/Si hybrid MOS optical modulator using a Si rib waveguide embedded in SiO_2, enabling low parasitic capacitance. In addition to narrowing the Si waveguide and optimizing the doping profiles as well as the n^+-InGaAs contact layer, the RC constant was improved by a factor of 21. As a result, we have achieved $V_\pi L$ of 0.37 Vcm with an EOT of 17.2 nm and a clear eye pattern at 12.5 Gbit/s, improving the trade-off relationship between $V_\pi L$ and modulation bandwidth. Since the further improvement in the modulation bandwidth is expected by process improvement, the presented III-V/Si hybrid MOS optical modulator is promising for realizing high-efficiency and high-speed optical modulation simultaneously.

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