Performance and Power of Soft-decision SDFEC for 100G -800G Applications

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Abstract: With the increase of traffic in coherent optical communication systems, the proportion of resources (chip area) required by FEC in DSP chips is higher and higher. At the same time, pre-FEC performance is an explicit indicator of commercial competition. It is gradually improved in the evolution of the system, and the Shannon limit is approached step by step. The balanced design of FEC performance, area, and power consumption becomes a key point of the DSP chip of coherent optical communication.

1. FEC design requirements for optical communication

The characteristics of high speed optical communication system have raised special requirements for FEC design. Firstly, the high throughput of the system requires FEC to perform a high parallelization of decoding implementations. Secondly, the requirement of 0 bit error transmission requires that the error floor of the FEC be at least 1e-15.Thirdly, the system raises different requirements for FEC coding delay, burst capability and decoding quantization bit width. Optical communication FEC undergoes the following developments: From hard decision to soft decision, from decoding to iterative decoding, from single-code to concatenated code, from packet code to convolutional code, from independent FEC to modulation and coding convergence. Currently, mainstream FEC schemes include: RS code, BCH code, TPC, staircase [1], LDPC [2], LDPCC [3], SCLDPC [4], SD-TPC [5], SD-staircase, etc. Many FEC can achieve performance of less than 1 dB of the Shannon limit, and basically have: Parallel implementation, low error layer, controllable decoding bit width, controllable iterative decoding times, and low delay (<5us in 100G throughput). Specific system application requirements are selected based on the specific requirements of performance, area, and power consumption.

2. Key Points Affecting FEC Performance and Complexity

The core reason why FEC can implement decoding performance is as follows: By adding an overhead bit to a certain length of information bits, a strong mathematical constraint relationship is formed between the information bit and the overhead bit. By using a constraint relationship, a certain quantity of errors can be corrected by decoding in a code length, thereby ensuring no bit error transmission of the system. The performance of FEC depends on the following points:

2.1 Coding and construction:

1) Constraints: Basic algebraic code solution of the FEC solution, for example: Parity check code, BCH code, RS code, etc.

2) Scope of the constraint: Code length. A longer code indicates better performance.

3) Times of the constraints: An information bit is restricted several times in a code length.

4) Grouping and convolution of constraints: Convolution relationship equivalent increases the code length.

2.2 Decoding

1) Decoding algorithm: Performance of obtaining external information; for example: obtain information outside the decoding based on a BP algorithm or a chase algorithm;

2) Number of times that an information bit is decoded. The value is equal to the number of iterations multiplied by the number of constraints.

3) Number of bits covered by one sub code decoding;

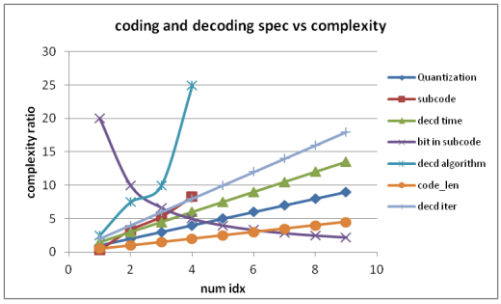
4) Decoding quantization bit width;

The following table compares the differences between soft decision LDPC codes and TPC as an example.

Table 1: compare of the encoding and decoding spec of LDPC and TPC

	LDPC	TPC
Code Spec	LDPC(18360,14688)	TPC(160,143)
Coding Constraints	Parity check code	BCH
Scope of the constraint	~20,000	~60,000
Constraints times	4	2
convolution	No	No
Decoding algorithm	BP	Chase
Decoding time	12iter*4layer	8iter*2layer
Bits in sub code	4	160
Quantization	4bit	bit
NCG	11.5	11.0
Power@14nm@100G	3w	1w

The factors that affect the performance are also the main factors that affect the complexity. In each single point of view, higher performance corresponds to more complexity. However, the specific FEC scheme is the combination of the foregoing multiple dimensions, and performance improvement and complexity increase of each dimension are not linear, but are the relationships shown in FIG. 1.



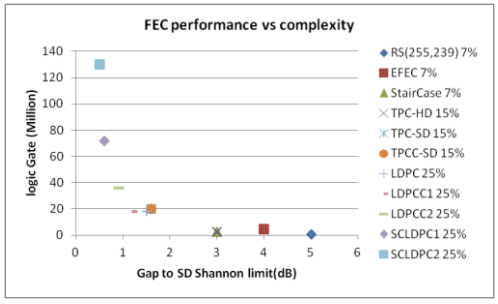


FIG. 1 coding spec vs complexity; FIG. 2 FEC performance vs complexity;

During the FEC solution design, the golden range of each dimension is selected to obtain the balanced design of the performance and complexity of requirements. Figure 2 shows the complexity of the current mainstream FEC scheme and it performance (distance to the Shannon limit).It can be seen that the relationship is not linear. When the Shannon limit is less than 1 dB, the performance improvement brings great complexity. In general, the power consumption of FEC is proportional to the complexity. However, the relationship between the power consumption and complexity of FEC is slightly different in actual optical communication systems. The main different is as follows:

1） In actual situations, the optical communication system works in 1.5dB~3db margin mode. For an iterative decoder, a large system margin is used, and a very little iteration times is required to enable the work to be started. For example, 25% convolutional LPDCC solution uses 12 iterations of @NCG 12 db. However, when the system works in the 1.5 dB margin system, the actual required decoding iteration times is 2~3 times. The decoder can design a dynamic

shutdown mechanism. In this case, the actual power consumption corresponds to only 2~3 iterations.

2） With the development of the ASIC process, the size of the component becomes smaller and smaller, the ratio of connections between components is higher and higher. Therefore, data transmission in the decoding process also brings about large consumption of power consumption. For example, the convolutional LDPC code with the same code length and the packet LDPC code are in the same decoding resource, because of the complex data transfer relationship, the convolutional codes increase the connection, which leads to the power consumption far higher than that of the packet LDPC codes.

3. Impact of Modulation and Coding Scheme on System Performance and FEC Complexity

New modulation and coding schemes, such as Constellation shaping, MLC, or 4D modulation, have been widely used in high-speed optical transmission systems. These solutions effectively improve system gains and flexibility, and greatly change FEC complexity and power consumption.

The constellation shaping solution [6] effectively improves the system performance, but the traffic of the FEC compilation code is also large. As shown in Figure 3, 400G 16Qam 25% fec. Different CS rates cause the increase of FEC compilation code traffic.

The MLC [7] solution applies to high-order modulation, which effectively reduces the traffic of soft decision FEC, but has a great impact on performance and system stability.

First, the tolerance capability of the MLC architecture for burst bit errors is greatly reduced. Compared with the standard gray coding, the capability of the hard decision decoding path is weak, resulting in a reduction of the system comprehensive burst error tolerance capability by nearly 4~8 times, which may also be understood as a cost of reducing complexity. Secondly, the MLC architecture has a different degree of tolerance reeducation in optical transmission system. The MLC solution reduces the FEC resources and also reduces the system stability.

4. Summary

With the increase of traffic in the high-speed optical communication system, the new modulation and coding scheme is widely used. How to select a FEC solution with relatively balanced performance and power consumption becomes the key to system design. At the same time, with the development of AISC technics, the compositions of power consumption of FEC also changes. This raises a new problem for the performance and power consumption balance design. This paper summarizes the key factors that affect the FEC performance and complexity. The system design can be considered to obtain the optimal solution design under the target performance.

Reference

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