Real-Time Demonstration of Silicon-Photonics-Based QSFP-DD 400GBASE-DR4 Transceivers for Datacenter Applications

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Abstract: We demonstrate a real-time silicon-photonics-based 400GBASE-DR4 transceiver packaged in a QSFP-DD form factor. The performance of the transmitter including TDECQ, extinction ratio and OMA and receiver sensitivity are measured, all satisfying IEEE 400GBASE-DR4 specifications. © 2020 The Author(s).

1. Introduction

Major datacenters have widely deployed 100G networks using four electrical and optical lanes (4x25G). Next-generation datacenter networks are expected to make heavy use of 400G. A high-performance and cost-effective optical interconnect solution is a critical part of the networks. The IEEE and industry multi-source agreements (MSAs) have specified a few different 400G optical transceiver technologies according to link media and distance, including 400G-SR8 (short reach), -DR4 (datacenter reach), -FR4 (far reach), and -LR8 (long reach), with respective link distance of 100 meters in OM4 multi-mode fiber (MMF), 500 meters in single-mode fiber (SMF), 1 km in SMF and 10 km in SMF [1]-[3]. 400G-DR4, which consists of four 100G optical lanes over four pairs of SMF fibers, is considered a most promising solution for 400G datacenter networks as it can be configured for 100G, 200G and 400G connections using optical breakout or shuffle cables, providing additional flexibility for network design.

Due to its small footprint, low power consumption, and compatibility with the CMOS eco-system, silicon photonics (SiPh) has become an attractive solution for datacenter interconnects [4]. SiPh-based 100G (4x25G) transceivers have been widely deployed, and bit rates per lane exceeding 100 Gb/s have already been demonstrated in research labs, using various modulation formats and FEC techniques [4]-[7]. However, no SiPh-based 400G transceivers have ever been reported. In this paper, we demonstrate 400G-DR4 transceivers in real-time operation based on SiPh technology and packaged in a QSFP-DD form factor [8].

2. Architecture of SiPh-Based 400GBASE-DR4 transceiver

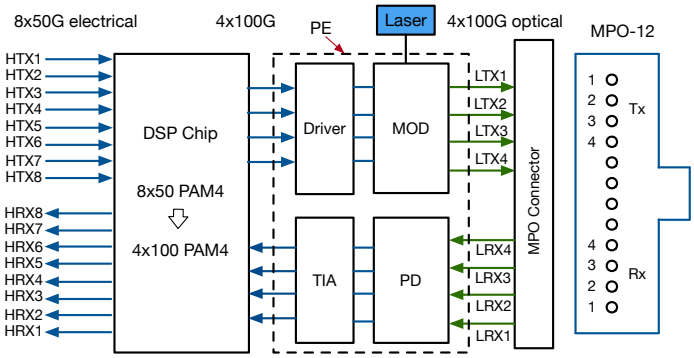


Fig. 1. Architecture of a SiPh-based 400G-DR4 transceiver. MOD: quad modulator, PD: quad photodiode, HTX: host-side transmitter, HRX: host-side receiver, LTX: line-side transmitter, LRX: line-side receiver, PE: photonic engine.

The architecture of the SiPh-based 400G-DR4 transceiver is depicted in Fig. 1, which has eight electrical inputs/outputs (I/O) denoted as HTX (host-side transmitter) and HRX (host-side receiver), each carrying a 26.5625-Gbaud 4-level pulse amplitude modulation (PAM4) signal. The DSP chip converts the 8 x 26.5625-Gbaud PAM4

signals to 4 x 53.125-Gbaud PAM4 signals, provides clock and data recovery (CDR) and performs equalization functions to compensate signal distortions caused by the electrical connection to the host switch and the transceiver itself. The four transmitter signals from the DSP are amplified by modulator drivers which then excite the SiPh modulators to produce 4 x 53.125-Gbaud PAM4 optical signals, which are denoted as LTX (line-side transmitter). On the receiver side, four lanes of optical signals, denoted as LRX (line-side receiver), are detected by photodiodes (PDs) and amplified by transimpedance amplifiers (TIAs). The resulting 4 x 53.125-Gbaud PAM4 signals are sent to the DSP chip for equalization, clock and data recovery, and converted back to 8 x 26.5625-Gbaud PAM4 signals. The optical I/O uses a Multifiber-Push-On-12 (MPO12) connector with 8 ports connected to fibers, as shown on the right of Fig. 1. As there are eight electrical lanes, the transceiver needs to be packaged in either a QSFP-DD or OSFP form factor and we use QSFP-DD packaging. In the transceiver, each two HTX/HRXs correspond to one LTX/LRX.

3. Photonic Engine

The Elenion 400G-DR4 chipset inside the photonic engine consists of a silicon photonic integrated circuit (PIC), two dual-channel modulator drivers, and two dual-channel transimpedance amplifiers (TIA). The monolithic PIC includes four parallel Mach-Zehnder modulators and high-speed photodiodes. The modulators and photodetectors each have 3-dB bandwidths in excess of 30 GHz and are DC-coupled to the driver and TIA chips, respectively. No external bias-T is necessary. The PIC also includes low-speed monitor photodiodes and optical phase control inputs. An array of edge couplers on the PIC directly interfaces with a butt coupled fiber array of SMF with 10-micron mode field diameters. A full custom DC-coupled 4-Vpp differential driver achieves >40-GHz bandwidth, 26-dB of gain, and better than 2% THD (total harmonic distortion). The custom designed low-noise linear TIA has 30-GHz bandwidth, 4k-Ohm transimpedance gain, and 600-mVpp output swing.

4. Real-Time Module Test

The test setup shown in Fig. 2a is for transmitter performance testing including eye-diagrams, Transmitter and Dispersion Eye Closure for PAM4 (TDECQ) and extinction ratios (ERs). In the test, an 8-channel 26.5625-Gbaud PAM4 bit-error-ratio tester (BERT) is used to generate eight independent pseudo-random-binary-sequence quaternary (PRBSQ) signals, which are sent to a QSFP-DD 400G evaluation board (EVB) and used as electrical input signals to DUT1 (device under test 1), a QSFP-DD 400G-DR4 module. To test the performance of each channel, the MPO12 cable is split into eight fibers with LC connectors. For measuring transmitter performance, each transmitter's output signal is sent through a 53.125-Gbaud CDR for clock recovery. The recovered clock is used by the 53.125-Gbaud Oscilloscope to generate eye-diagrams, TDECQ and ER measurements. Due to the optical splitter in the CDR, the optical power entering the DCA is 4.4 dB lower than exiting LTX.

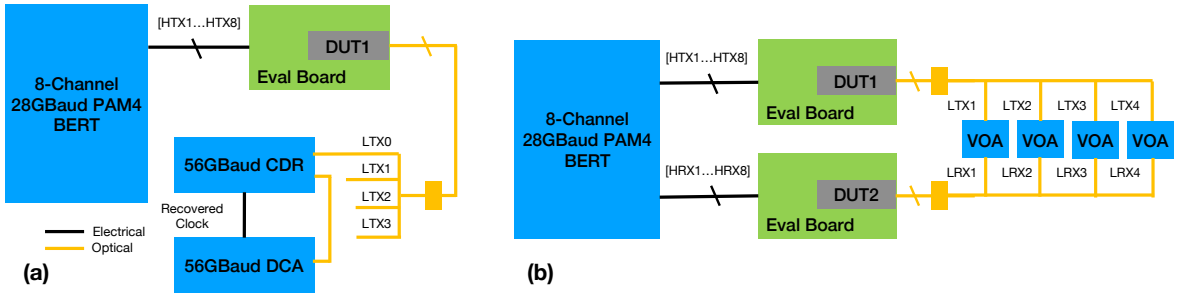
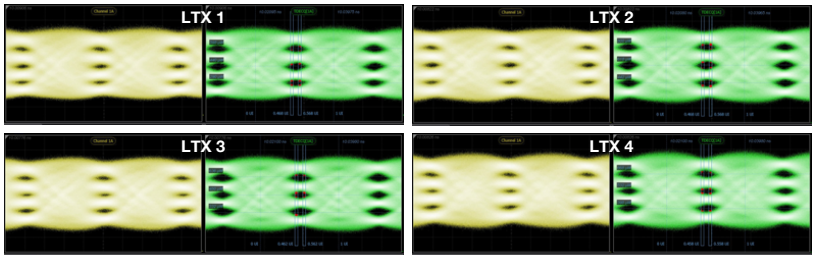


Fig. 2. Test setups. (a) Transmitter performance test, (b) system performance test. HTX: host-side transmitter, LTX: line-side transmitter, HRX: host-side receiver, LRX: line-side receiver

Fig. 3 shows the measured transmitter optical eye-diagrams, TDECQs, ERs and optical modulation amplitudes (OMAs) of all four channels of DUT1. In this measurement, PRBS15Q signals are used. For each transmitter eye-diagram, the left one is the raw eye-diagram and the right one the eye-diagram after the TDECQ reference equalizer, a 5-tap, T-spaced, feed-forward equalizer (FFE) specified by IEEE [1], where T is the symbol period. All four channels have open raw eyes, and the eye-diagrams after the reference equalizer are improved of course. TDECQs of all the four channels are lower than 2.5 dB, ERs are larger than 3.5 dB, and the OMAs of all channels are over 0 dBm, better than the IEEE specifications [1].

To test receiver sensitivity, two QSFP-DD 400G EVBs are used, each with a DR4 transceiver, shown in Fig. 2b. DUT1 in this measurement is an Electro-absorption Modulated Laser (EML)-based transceiver using only one transmitter, LTX2, as a reference transmitter with HTX3 and HTX4 electrical signals from the BERT. The second

EVB hosts DUT2, a tested SiPh DR4 module, as a receiver with all eight HRX electrical signals connected to the BERT. The LTX2 output, through a variable optical attenuator (VOA), is sequentially connected to each LRX of DUT2. The BERs are measured on the host electrical channels with PRBS31Q signals transmitted. Fig. 4a shows each BER vs. OMA curve, where HRX1 and HRX2 correspond to LTX1, HRX3 and HRX4 corresponding to LTX2 and so on. It shows that all channels can reach a BER of about 10^{-8}. The performance difference between channels is caused by sub-optimal settings of each receiver, which can be further adjusted but will take some time. The receiver sensitivity is defined as the OMA at which the BER exceeds $2.0\text{x}10^{-4}$, the threshold of the DR4 FEC (forward error correcting) [1]. The receiver sensitivities of all channels are better than -4.4 dBm, reaching the IEEE specifications. B2B 400G transmission performance is next measured for two SiPh DR4 modules, one as transmitter, the other as receiver as shown in Fig 2b. Two MPO12-to-LC breakout cables are used and the input optical power to each channel of DUT2 is adjusted with a VOA. The results are illustrated in Fig. 4b. Clearly BERs of all the channels are under the FEC threshold and the link has a good power margin. It is expected that with further optimization of transmitter and receiver settings, the performance difference between channels can be reduced.



	TDECQ (dB)	ER (dB)	OMA (dBm)
LTX1	2.19	5.00	1.18
LTX2	2.15	4.09	1.77
LTX3	2.28	4.40	0.88
LTX4	2.29	3.65	0.59

Fig. 3. Measured transmitter optical eye-diagrams and TDECQ of DUT1

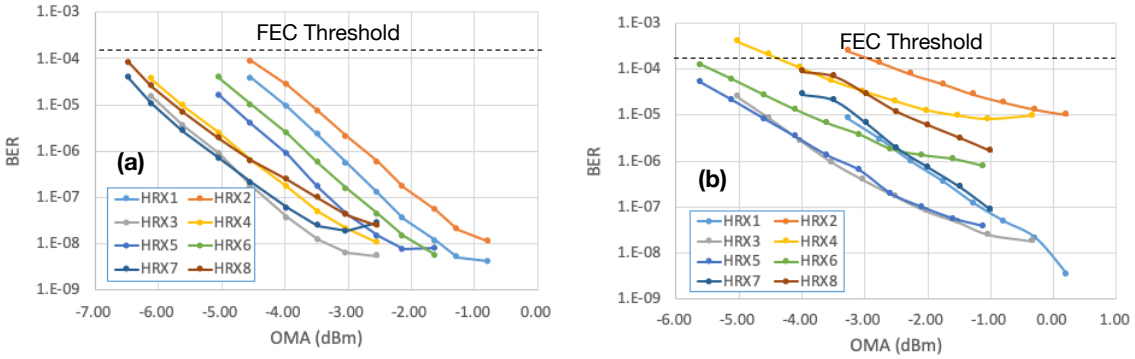


Fig. 4. (a) Received BER of each channel of DUT2, one at a time, with optical signal from a reference LTX, (b) B2B transmission performance of all four channels from one module to another (DUT1 to DUT2).

4. Conclusions

In conclusion, we have demonstrated SiPh-based 400G-DR4 transceivers packaged in a QSFP-DD form factor. The real-time transmitter performance such as TDECQ, ER and OMA, and receiver sensitivity are all better than IEEE specifications. B2B performance shows that all channels work under the DR4 FEC limit with a good margin.

5. References

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