45nm CMOS - Silicon Photonics Monolithic Technology (45CLO) for next-generation, low power and high speed optical interconnects

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Abstract: GLOBALFOUNDRIES' monolithic 45nm CMOS-Silicon Photonics 300mm high-volume manufacturing platform based on 45nm RF technology node, and optimized for high performance and low power short-reach optical interconnects for on-chip and chip-to-chip applications will be discussed.

OCIS codes: (130.3120) Integrated optics devices; (250.3140) Integrated optoelectronic circuits; (130.1750) Components; (250.5300) Photonic integrated circuits.

1. Introduction

A competitive 90nm CMOS-silicon photonics foundry technology [1], offered by GLOBALFOUNDRIES, has been scaled to the new monolithic silicon platform based on the 45nm RFCMOS technology node. This advanced 45CLO technology provides the best in class silicon photonics devices currently operating at C and O-bands. This platform allows for tight and seamless integration of electronic circuits and photonic devices in order to enable a low-cost, mass production, and high-performance optical transceiver pushing the single lambda modulation speed up to 100Gbaud. In this paper, we will discuss the performance of the silicon photonics and CMOS devices as well as explain how monolithic integration of electronic circuits with optical devices enables modulation speed boost while simultaneously maintaining low power consumption.

2. Platform Overview

This technology offers monolithic integration of high quality active and passive silicon photonics devices with high f_T CMOS transistors by utilizing dual silicon thicknesses and dual contact modules (CA and CB in Fig. 1a). GF silicon photonics platform (45CLO) is built on a 300mm SOI wafer with 160nm thick top silicon and 2µm thick buried oxide, and the SOI is thinned to 88nm in the CMOS region to achieve CMOS device performance approaching that of GF 45RF technology. Optical silicon devices based on GF 90WG technology is built on a 160 nm thick SOI. The passive device offerings include fully etched ridge waveguides (RX), partially etched 50nm slab waveguides (KG) and multimode silicon waveguides. In 45CLO, we additionally offer an ultra-low loss 300nm thick SiN waveguide (Fig. 1a). Currently the active devices in 45CLO support up to 56GBaud symbol rates and efforts are ongoing to enable new modulators to further improve the speed.

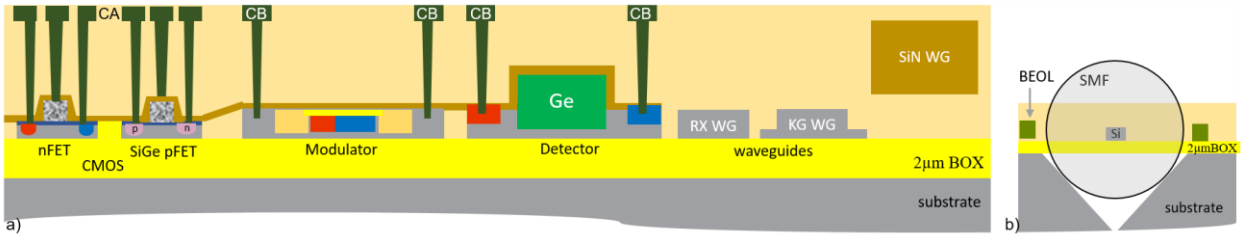


Fig. 1. (a) Cross-section showing front end and middle of line of 45CLO technology.
(b) Cross-section diagram of the IOSMF with v-groove and the attached fiber.

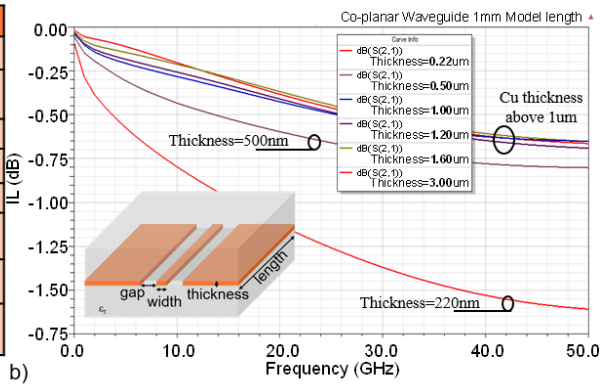
Fig. 2a compares the CMOS performance of the 90nm silicon photonics (90WG) technology to the 45RFSOI and 45CLO technologies. The 45CLO technology offers significantly improved CMOS devices with an RF friendly, 8-metal layer stack back-end. The first five copper metal layers are suitable for complex logic circuits. The top two metal layers include a 1.2µm thick copper, and a 1.2µm aluminum for routing low loss transmission lines (Fig. 2b), and building high-Q inductors. The 45CLO platform also offers an advanced IOSMF coupling solution, the self-

aligned v-groove and spot size converter have been improved to offer a lower loss solution for fiber or fiber array attachment providing robust, high-performance and high-yield optical coupling (Fig. 1b). GF 45CLO technology leverages state-of-the-art CMOS and silicon photonics design kit (PDK) with EO co-design environment including comprehensive C and O-band device library (L-band in roadmap), compact models, waveguide routing tool, LVS and DRC tools.

	90WG SiPh	45RFSOI	**45CLO SiPh**
Mask count	51	40	59
Tsi SOI / Box thickness (nm)	160 / 2000	88 / 200	88 /2000 CMOS 160/2000 Photonic
Contacted Gate pitch (nm)		190	250
Nominal Supply (V)	1.2V / 2.5V	1.0V / 1.8V	1.0V / 1.8V
Min Phys Gate Length (nm)	55	41	41
Monolithic CMOS	RVT,LVT,DG (3.3V)	RVT,UVT, AVT,DG(1.8V)	RVT, UVT, AVT, DG (1.8V)
NFET Peak f_T/f_{MAX} (GHz) target	148 / 224	300 / 355	* 280 / 340
PFET Peak f_T/f_{MAX} (GHz) target	~80/	245 / 305	* 230 / 290 with eSiGe

* SiPh integration impacts

a)

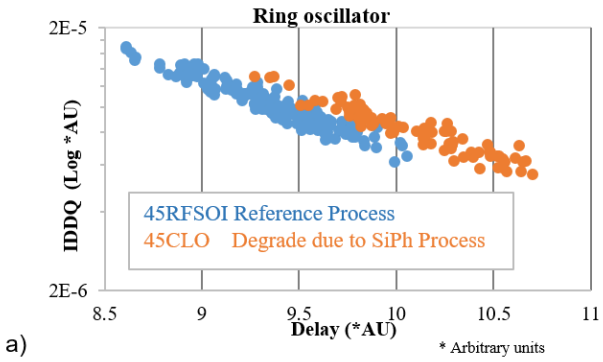


b)

Fig. 2. (a) 45CLO CMOS technology comparison to the parent RF reference node: 45RFSOI and CMOS-SiPh 90WG node. (b) The simulated insertion loss of a 1mm long coplanar GSG transmission line for different conductor thicknesses.

3. CMOS and Optical device performance

The primary advantage of the 45CLO platform is to offer 45RF CMOS performance while still providing state of the art photonic devices. In order to accomplish this, significant process optimization was done to mitigate the impact on the CMOS devices and some of the active photonic devices, such as Germanium photodiode. As an example, Fig. 3a highlights the CMOS performance to be within 7% of the target device while keeping the high-performance characteristics of the photodiode.



a)

Parameter	90WG Targets	45CLO O-Band
350 nm SOI (RX) waveguide loss	1.7 dB/cm	1.36 dB/cm
810 nm SOI multimode wg loss	0.8 dB/cm	0.59 dB/cm
SiN waveguide loss	n/a	0.35 dB/cm
SOI 10 µm bend loss	0.0095 dB/bend	0.007 dB/bend
WIC 50:50 coupler loss	0.09 dB/device	0.049 dB/device
PSR TE/TM output loss	0.19 /0.6 dB/device	0.22 / 0.4 dB/device
MZI 3dB BW (-2 V DV)	35 GHz	35 GHz
GePD (EPI 0.7 µm)	>0.9 A/W	0.9 A/W
GePD 3dB BW (EPI 0.7 µm)	39 GHz	50 Ghz
GePD Idark (EPI 0.7 µm)	< 40 nA	<40 nA
IOSMF Loss TE/TM (ORL)	-0.9/-1.5 (-30) dB	-0.8/-1.5 (-30) dB

b)

Fig. 3. (a) Measured insertion distribution of the OFF-state leakage current IDDQ as a function of ring oscillator delay. (b) Compares the 90WG active and passive silicon photonics device performance to the 45CLO technology.

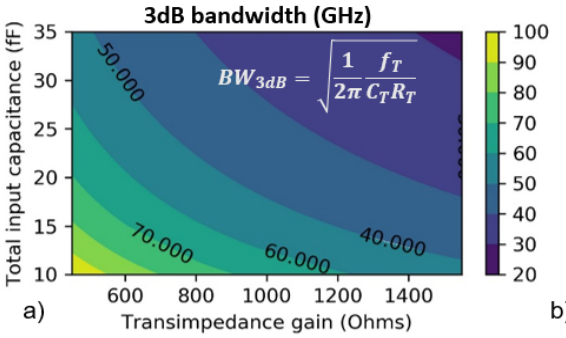
In Fig. 3b, the performance of optical devices are benchmarked against the 90WG silicon phonics technology [1]. The data shows comparable or better optical performance for all of 45CLO devices. The improvement in waveguide loss is achieved by implementing (1) advanced immersion 193nm lithography for both the RX and KG waveguides as well as by (2) moving to a high density design grid. The 45CLO Ge photodiode also shows significant improvement in performance due to the alternative heat cycles as shown in Fig. 3b.

4. Value of 45CLO monolithic CMOS – Silicon Photonics platform

Another advantage of 45CLO monolithic integration is to reduce the complexity and cost of packaging. Unlike the hybrid integration of electronics circuitry and silicon photonics devices using advanced 2.5D or 3D die stacking techniques, only the monolithic approach can offer truly parasitic-less integration. The parasitics and the capacitive load on the interface between active photonics devices (modulators or photodetectors) and their control electronics (drivers and trans-impedance amplifiers) has a tremendous impact on overall system performance. Low power, optical hybrid integrated CMOS-SiPh transceivers, as demonstrated by [2-4], rely on available foundry logic transistors to interact with photonics devices. This allows them to achieve a modulation speed up to 40-56Gbaud, maintaining

moderate power consumption to be competitive with conventional copper-based interconnects. However, in many cases of hybrid integration, the choice of CMOS technology is driven by the functionality of electronic die (DSP, CPU/GPU, Memory or switches) which is not necessarily optimized for photonic transceiver applications.

In order to illustrate the benefits of monolithic integration, we discuss the transmitter and receiver separately. Silicon photonics modulators require a typical driving voltage around 1.5V-2.5V [5, 6], which is higher than a core logic supply. Unlike in BULK, SOI technology allows area efficiency by transistor stacking to achieve a required voltage swing. The advanced, high-speed modulators such as Micro-Ring-Modulators (MRM) [5] or Electro-Absorption-Modulator (EAM) [6], typically represent a load for the drive at the range of 20-50fF, which could be comparable with the parasitic capacitance present on the interface between CMOS and SiPh die - in the hybrid integration scheme. In monolithic integration, on the other hand, there is no such parasitic load; hence, the driver power efficiency, as well as total modulation speed, can be significantly improved.



b)

	14nmFF	22FDX	CMS90WG	45CLO
NMOS f_T	270GHz	350GHz	150GHz	**280GHz**
Supply Voltage	0.8V	0.8V	1.2V	**0.9V-1.1V**
Technology	BULK	SOI	SOI	**SOI**
Mx res and cap	high	low	very low	**very low**
Integration	hybrid	hybrid	monolithic	**monolithic**
- Parasitic load	5-30fF	5-30fF	0	**0**
- ESD diode	~50fF	~50fF	0	**0**
Expected/Estimated NRZ bitrate	40-50 Gb/s [2-3]	>60Gb/s	up to 50Gb/s	**up to 100Gb/s**

Fig. 4. (a) Analytical receiver 3dB bandwidth (GHz) estimation of 4CLO technology (transistor f_T=280GHz) in the function of total input capacitance C_T and gain R_T. (b) CMOS technology comparison for low-power silicon photonics transceiver applications.

Even a stronger impact on the system performance can be observed on the optical receiver, where the 3dB bandwidth of the trans-impedance amplifier (TIA) strongly depends on the total input capacitance (Fig. 4a). In monolithic 45CLO technology, there are no parasitic capacitances between the photodetector and the TIA. Besides, the total input load can be further reduced by removing the ESD protection because in monolithic integration schemes, the transistors gates do not need protection. Therefore, the total input capacitance of the monolithically integrated receiver could be at range of 20fF, including photodiode, TIA input stage and metal interconnect.

Even though the transistor speed, measured by the f_T parameter, in the 45CLO technology is comparable to the 14nm FinFET, the achievable modulation speed of 45CLO is expected to be twice that of 14nm FinFET for optical transceiver applications. Owning to the monolithic integration of silicon photonics and CMOS devices as well as the RF friendly back-end (high f_{max}), the superiority of the 45CLO technology for short-reach optical interconnects in comparison to hybrid approach, is summarized in Fig. 4b.

5. Conclusion

GLOBALFOUNDRIES 45CLO technology enables efficient integration of RF transistors with best in class silicon photonics devices providing the high volume and low-cost solutions for package-to-package or chip-to-chip optical transceivers fulfilling high bandwidth density and low-power requirements for next-generation systems.

6. Acknowledgment

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5. References

[1] Giewont, Ken, et al. "300-mm Monolithic Silicon Photonics Foundry Technology." IEEE JSTQE 25.5: Pg. 1-11 (2019).
[2] Rakowski, M., et al. "Hybrid 14nm FinFET-Silicon Photonics Technology for Low-Power Tb/s/mm 2 Optical I/O." 2018 IEEE VLSI, (2018)
[3] Raj, Mayank, et al. "A 50Gb/s Hybrid Integrated Si-Photonic Optical Link in 16nm FinFET." 2019 Symposium on VLSI Circuits. IEEE, (2019)
[4] Atabaki, Amir H., et al. "Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip." Volume and page. Nature (2018).
[5] Ban, Yoojin, et al. "Low-Voltage 60Gb/s NRZ and 100Gb/s PAM4 O-Band Silicon Ring Modulator." 2019 IEEE Optical Interconnects Conference (OI), IEEE, (2019).
[6] Ramon, Hannes, et al. "70 Gb/s Low-Power DC-Coupled NRZ Differential Electro-Absorption Modulator Driver in 55 nm SiGe BiCMOS." Journal of Lightwave Technology 37.5 Pg 1504-1514 (2019).