# 400G Silicon Photonics Integrated Circuit Transceiver Chipsets for CPO, OBO, and Pluggable Modules

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**Abstract:** 400G-FR4 silicon photonics transmit-receive chipsets, compatible with co-packaged-optics, on-board-optics, and pluggable form factors, were demonstrated with a combined bandwidth density of 94Gb/s/mm, energy efficiency of <10pJ/bit, and -5.4dBm OMA sensitivity at the KP4 pre-FEC-BER=2.4e-4.

**OCIS codes:** (130.3120) Integrated optics devices; (250.3140) Integrated optoelectronic circuits; (130.1750) Components.

## 1. Introduction

Electrical and optical transceiver data rates inside datacenter and accelerator clusters are increasing to keep up with rapidly growing traffic demand due to the rise of 5G, IoT, and AI applications. At 100G/lane (e.g. 50Gbaud PAM4) and higher, the electrical interfaces of processors (i.e. Switch, FPGA, CPU, GPU, etc.) become energy inefficient due to increased RF propagation losses inside the package and along the traces connecting the package and the optical transceiver modules plugged on to faceplate, limiting the bandwidth growth. The 12.8Tb/s switch ASIC used in today's switch racks connects 256 lanes of 50Gb/s electrical interfaces to 32 QSFP56-DD (e.g. 400G-DR4 IEEE 802.3bs or 400G-FR4 100G Lambda MSA) modules. The modules fill up the 1RU chassis faceplate with a bandwidth density of 22Gb/s/mm and consume an energy of 37.5pJ/bit (Fig. 1(a)) [1].

To continue the bandwidth scaling, next-generation switch ASICs will have 106Gb/lane electrical interfaces that require on-board energy-hungry re-timers or long-range SerDes interfaces or expensive breakout copper cables to connect to optical transceiver modules at the faceplate. These options do not maintain the form factor, energy density, power, and cost and are therefore not desired. The solution is to reduce the electrical interface power consumption by bringing optical transceivers inside the chassis closer to processors initially as on-board optics (OBO) and ultimately as co-packaged optics (CPO) form factors [2,3]. The CPO form factor brings challenges of package size, bandwidth density, energy consumption, and reliability to optical transceivers. CPO transceivers and switch ASIC will share a single organic package that is limited to a 90mm×90mm footprint due to manufacturing challenges (Fig. 1(b)). Assuming 4 sides of the package will be used to escape bandwidth out of a 25.6 or 51.2Tb/s switch ASIC with CPO transceivers, each side will carry 6.4 or 12.8Tb/s data transfer over a 70mm or less edge of the package, requiring an ultra-high bandwidth density above 90Gb/s/mm. Also, the power consumption of CPO transceivers needs to be maintained below 500W at 51.2Tb/s to use non-exotic cooling methods, requiring an energy consumption of less than 10pJ/bit. In addition, the CPO transceivers are required to operate at or above 85°C similar to ASICs, which requires to move lasers away from the transceiver to an external/remote location.

Here, we introduce 400G-FR4 compliant Silicon Photonics Integrated Circuit (PIC) transmit and receive chipsets that offer a combined bandwidth density of 94Gb/s/mm and an energy efficiency of <1pJ/bit PIC and <10pJ/bit combined with RFICs, digital interfaces and bias and control circuitries in transceiver optical sub-assemblies (OSA) (Fig. 1(a)). The compact form factor and ultra-low energy consumption are achieved through the integration of athermal CWDM4 MUX and DEMUX filters, low-voltage optimized modulators, and polarization diversity detectors that all were operated at or above 85°C. When OSAs were connected to a merchant 100Gb/lane PHY as a

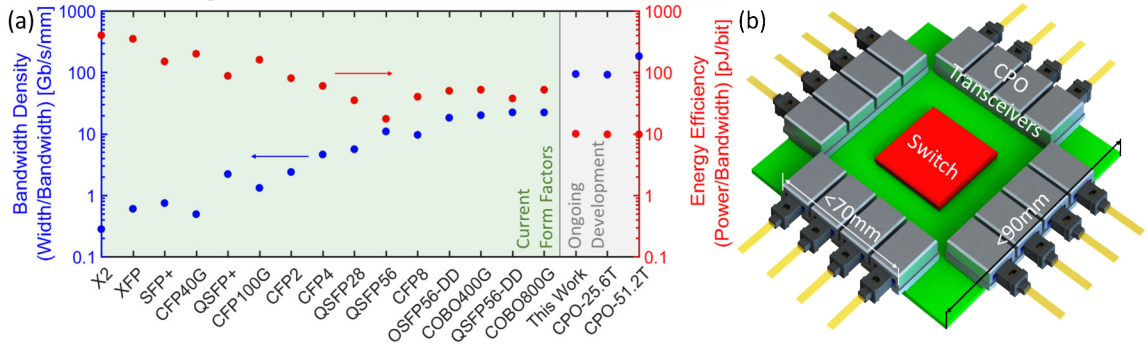


Figure 1. (a) Bandwidth density and energy efficiency of all optical form factors with comparison to 400G-FR4 chipsets in this work. (b) 3D sketch of CPO transceivers and switch package with assumptions of physical dimensions and transceiver placement.

proxy to the Switch SerDes, a KP4 pre-FEC BER of 2.4e-4 was measured for 100GbE packets with a -5.4dBm optical modulation amplitude sensitivity. Therefore, PHY power is excluded from the transceiver energy calculation. Given these specifications, these chipsets are compatible with CPO, OBO, and pluggable form factors.

## 2. 400G Silicon PIC Building Blocks

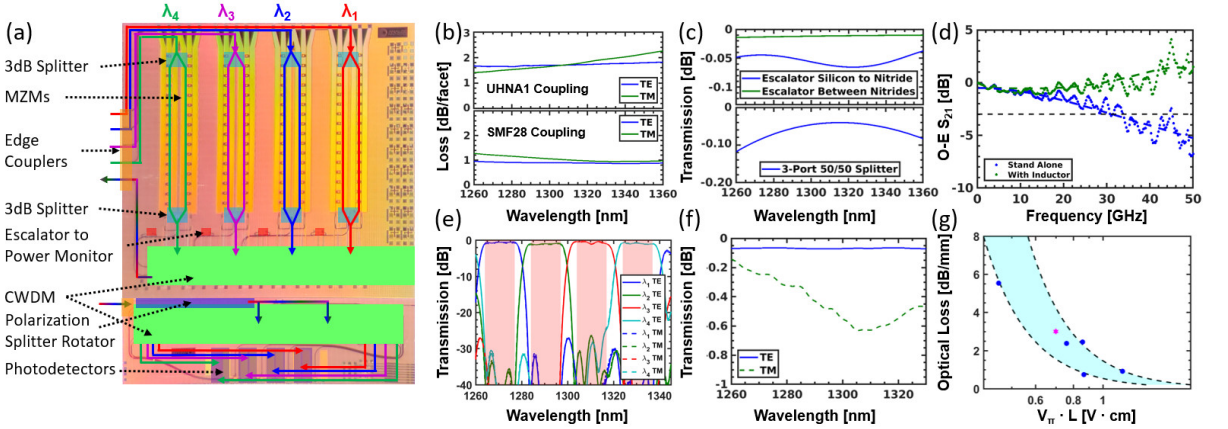


Figure 2. (a) 400G-FR4 Silicon Tx and Rx PIC die images and block diagram. (b) Coupling efficiency of the edge couplers to UHNA1 and SMF28 fibers. (c) Transmission spectra of escalators and 3dB splitters. (d) Photodetector bandwidth with and without on-chip inductors. (e) Transmission spectrum of CWDM4 (DE)MUX filters measured for both polarizations. (f) Transmission spectrum of polarization splitter rotator. (g) Measured optical loss vs. VπL (blue dots and star (used in demonstrator)) and design space (shaded blue area) of AP MZMs.

The 400G-FR4 silicon PIC transmit and receive chipsets and component level building blocks are shown over the die images in Fig. 2(a). The chipsets occupy a combined width of 4.26mm and bandwidth density of 94Gb/s/mm. All components were optimized to achieve the best-in-class link and power budgets. The fiber-to-chip couplers can easily limit the link budget of silicon photonics transceivers. The technical challenge is to expand the highly confined silicon waveguide modes to standard single-mode fiber modes (MFD~9um) to achieve high mode overlaps and impedance matching. Vertical/grating couplers are typically used to emit over an area matching to the mode size but the low tolerance to fabrication and temperature variations, and narrow bandwidths limit their coupling efficiency over O band (1260nm to 1360nm). Here, we developed low-loss edge couplers and the 400G-FR4 chipsets include an optimized edge coupler with a coupling efficiency of <1.5dB loss/facet to UHNA1 single-mode fiber. This fiber was then efficiently spliced (<0.5dB/loss) to an SMF28 fiber over the O band (Fig. 2(b)). We also demonstrated an optimized edge coupler with a coupling efficiency of ~1dB/facet directly to SMF28 fibers for both polarizations over O band. At present, these couplers are being combined with the rest of the PIC building blocks to reduce alignment tolerance, optical loss, and packaging cost (Fig. 2(b)). The escalators (i.e. layer transitions) between the silicon and silicon nitride waveguides and 3-port splitters used in MZMs were all demonstrated with <0.1dB loss over O band (Fig. 2(c)). The receiver PIC includes a photodetector (PD) with ~35GHz bandwidth and responsivity of >0.9A/W, capable of receiving 53Gbaud PAM4 signal (Fig. 2(d)). The PD bandwidth can be also extended over 50GHz with an integrated inductor, making it suitable for 100Gbaud transceiver applications.

To enable on-chip coarse wavelength division multiplexing and demultiplexing of the 4 channels, we developed passive athermal (DE)MUX CWDM4 filters integrated with active and passive PIC building blocks. A typical response of the CWDM4 filter is displayed in Fig. 2(e), providing a flat-top and low loss response while maintaining a <-25dB channel crosstalk across a 14nm channel bandwidth, exceeding the FR4 standard (i.e. 12nm). Furthermore, a polarization splitter rotator (PSR) is required to provide polarization diversity. The PSR was demonstrated with ~0.1dB loss for the TE polarization and <0.6dB loss for the TM polarization, leading to a PDL of <0.5dB (Fig. 2(f)). The MZM phase shifters were designed and measured to have both low VπLs and optical losses (Fig. 2(g)). To minimize power consumption, the phase shifter with <0.7V·cm and 3dB/mm loss was chosen while maintaining traveling wave characteristics for high bandwidth operation, resulting in <1pJ/bit with 2VppD drive [4].

## 3. High-Temperature Operation

The silicon PIC transceiver's tolerance to high and varying temperature conditions is essential to operate in an uncooled environment, especially in the CPO form factor. The most temperature-sensitive components are the MZM, photodetectors, and CWDM4 (DE)MUX filters. Therefore, we monitored the performance of these components against varying temperature conditions. Fig. 3(a) shows the Mach-Zehnder modulator eye diagrams from RT to 110°C. From 23˚C to 110˚C, eye quality factor and extinction ratio were maintained while using a closed-loop feedback to lock the MZM at the bias point, verifying temperature insensitive operation. To verify the high-temperature performance of the photodetector, the dark current was measured across the wafer, shown in Fig.

3(b). An increase of dark currents was observed over the temperature, increasing the shot noise. However, the shot noise remained below the thermal noise and did not impact the receiver sensitivity.

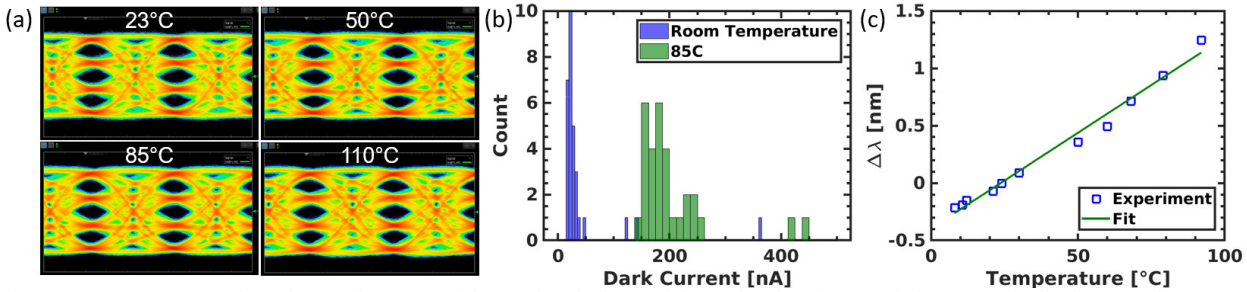


Figure 3. (a) Temperature dependent performance of the Mach-Zehnder modulator. (b) Photodetector dark current distribution over the 300mm wafer at room temperature and 85˚C. (c) Temperature dependence of CWDM4 filter, showing a channel wavelength dependence of 15pm/˚C.

A regular uncooled datacom laser wavelength can detune at a rate of 0.15nm/˚C to the ambient temperature. Due to this detuning, the wavelength division multiplexer should have a channel bandwidth of 12nm according to FR4 standard over the temperature range of 0 to 70˚C. Figure 3(c) shows the wavelength shift of the CWDM4 filter to the temperature, demonstrating a detuning rate of 15pm/˚C or <±0.6nm over a ΔT=85˚C. Given the initial 14nm flat-top response of the CWDM4 filter, the filter maintains the required bandwidth of 12nm over temperature.

## 3. 100GbE/λ Demonstration

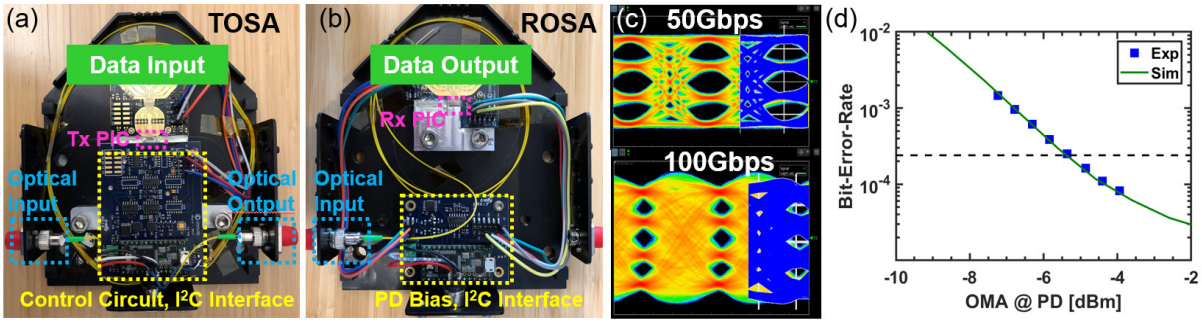


Figure 4. (a) Transmit and (b) Receive optical sub-assembly (TOSA and ROSA) evaluation box images. (c) Measured and modelled 50Gb/s and 100Gb/s PAM4 eye diagrams of the TOSA and ROSA transceiver. (d) 100GbE/λ Pre-FEC Bit-Error-Rate (BER) vs. optical modulation amplitude at the photodetector of the TOSA and ROSA transceiver, obtained with a 100GbE/lane PHY.

To test compatibility with 400G-FR4 MSA, transmit and receive optical sub-assemblies (TOSA and ROSA) were assembled by wire bonding the Analog Photonics Tx and Rx PICs directly to commercial-off-the-shelf (COTS) quad TIA and to high-speed chip-on-boards that include COTS quad driver. The edge couplers of the PICs were then attached to UHNA1 fibers that were spliced to SMF28 fiber interfaces. The modulators, drivers and TIAs were then connected to a DC board that includes control circuitry for locking to the quadrature, $I^2C$ interfaces to communicate with RFIC, and bias voltages to PDs and MZMs (Fig. 4(a) and (b)). After the final assembly, TOSA and ROSA were then connected through a 2km fiber to form the 100G-FR and 400G-FR4 optical communication links. The TOSA was driven with 50Gb/s and 100Gb/s digitally equalized <0.8VppD signal from Keysight AWG M8195A pattern generator and open eye diagrams were recorded at the ROSA output with Keysight DCA 86100D scope, agreeing well with system models (Fig. 4(c)). The TOSA and ROSA were then connected to a COTS 100GbE/lane PHY which passes ethernet packets and records the pre-FEC Bit-Error-Rate (BER) at 106Gbps (100GbE) data rate. An optical modulation amplitude (OMA) sensitivity of -5.4dBm was measured on the PD at KP4-FEC BER limit of 2.4e-4 (see Fig. 4(d)). The total energy consumption was recorded during the tests and did not exceed 10pJ/bit or 4W at 400Gbit/s.

## 4. Conclusion

We have designed and developed 400G-FR4 Silicon Photonics transmit and receive chipsets, compliant with IEEE 802.3bs and 100G Lambda MSA standards. To the best of our knowledge, we demonstrated a record high bandwidth density of 94Gb/s/mm and an energy efficiency of <10pJ/bit. Our solution provides excellent compatibility with current state-of-the-art pluggable optics modules, OBO, and future CPO form factors.

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