1.6Tbps Silicon Photonics Integrated Circuit for Co-Packaged Optical-IO Switch Applications

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Abstract: We demonstrate 1.6Tbps Silicon Photonic Integrated Circuit (SiPIC) meeting co-packaged optics requirements for network switch applications. The SiPIC has sixteen 106Gbps PAM4 optical channels, including lasers, modulators and V-grooves. Post-FEC error-free operation over temperature is demonstrated.

OCIS codes: (130.3120) Integrated optics devices; (140.3290) Laser arrays; (130.4110) Modulators

1. Introduction

Data center IP traffic is doubling every 2.5 years, driving the need to double Ethernet switch and connectivity bandwidths on a similar cadence [1]. While pluggable optics have been able to scale and keep pace with the associated interconnect demands, it is generally accepted that co-packaged optics will be needed to enable future scaling. In fact, the prevailing view is that this paradigm shift could take place within the coming five years, to intercept the 51.2 Tbps switch node, if not earlier. Co-packaged optics, for this particular application, will shrink the optics that are on the front plate and place them inside the switch blade, directly on the same package as the switch ASIC [2-4]. This new architecture enables significant SERDES and overall power reduction as the electrical channel between switch and optics now shrinks to tens of millimeters in length, and alleviates front panel physical congestion because the bulky pluggable modules are now replaced by simple fiber patch panels. We report here the demonstration of a fully integrated 1.6 Tbps silicon photonics integrated circuit (SiPIC) to enable co-package optics. It comprises x16 1310nm optical channels, each capable of 106 Gbps PAM4 performance. It is designed for small footprint, superior laser reliability, low-cost passive fiber array alignment, and low power consumption. This SiPIC will be the core optics for 1.6 Tbps photonic transceivers or photonic engines (PE), which can be assembled in groups of 16 around a 25.6 Tbps Ethernet switch ASIC to enable the co-packaged optical-IO switch IC system described above and shown in Fig. 1(a). This paper presents details of SiPIC components for 1.6Tbps SiPIC, fabricated using Intel's Silicon Photonics Technology.

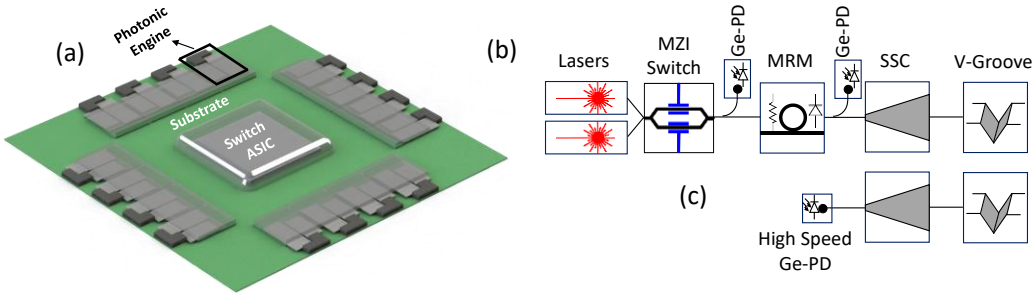

Fig. 1. (a) A 3-dimensional drawing of the integrated co-packaged optical IO switching system Schematic of 25.6 Tbps switch package with sixteen 1.6Tbps photonic engines. SiPIC architecture for each of 16 integrated Tx (b) and Rx (c) channels.

2. SiPIC Design and Results

Fig. 1(b) and (c) show Tx and Rx channel architecture within 16-channel SiPIC, respectively. On the Tx side, we used 32 hybrid distributed feedback (DFB) lasers, two lasers per channel. The redundant lasers in our platform came with no extra cost and improve on the FIT rate of a switch package with 256 integrated lasers. Subsequently we used Mach-Zehnder (MZ) switch to select between each of the two lasers. The laser light then was modulated using high-speed and compact micro-ring modulator (MRM) that has integrated metal heaters to control the resonance of the ring and two integrated Ge-photodetectors (PD) to individually determine MRM bias point insertion loss (IL) and

control. The modulated light then was converted to 9um mode field diameter using integrated spot size converter (SSC) that are integrated with V-grooves within lithographic tolerances, to allow for high volume and low loss passive alignment of SMF28 fiber with SiPIC. On the Rx side, the incoming light is coupled into SiPIC using V-grooves and polarization insensitive SSC and then directed to integrated high speed Ge-PD.

The DFB lasers are fabricated using Intel's hybrid silicon laser platform, as described in [5-7], where un-patterned III-V dies are bonded to a silicon-on-insulator (SOI) wafer already patterned with optical waveguides and Bragg gratings. Further processing is done to define the laser mesa, contacts, and III-V tapers to couple the light from the laser to the silicon waveguide. An example of laser output power coupled to the silicon waveguide vs. bias current and voltage vs. bias current is shown in Fig. 2(a) and (b) at 40C, 60C, and 80C. The laser provides more than 20mW with less than 220mW power consumption at 80C. The required bias current for 20mW output power at 80C increases less than 5% after highly accelerated life testing equivalent to 20 years of life at use condition. Design and process optimization should further improve laser efficiency and power consumption. High side-mode suppression ratio (SMSR) of greater than 45dB measured at 25C and 130mA operating current and low relative intensity noise (RIN) of less than -145dB/Hz measured at 25C and 60mA are collected on fully integrated SiPICs and demonstrated across all transmitter channels with redundant lasers as shown in Fig. 2(c) and (d), respectively. The IEEE 802.3-bs specifications for SMSR and RIN for 100Gbps links are shown in red, as reference.

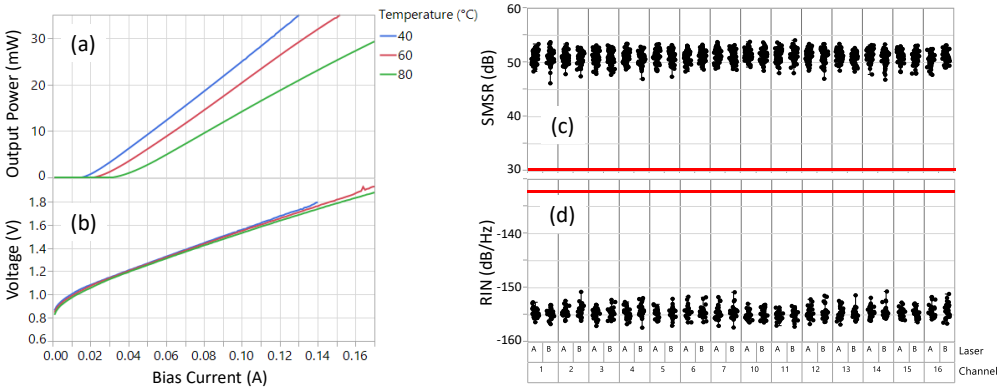

Fig. 2. (a) LI and (b) IV of an integrated hybrid III/V laser at 40, 60 and 80C. (c) SMSR at 25C and 130mA and (d) average RIN at 25C and 60mA for each of the 16 transmitter channels with redundant lasers A and B, across a 300mm wafer.

We also integrated Ge-PDs within the same SiPIC platform, in order to achieve low dark current, high responsivity and high bandwidth detector within our integrated platform. The Germanium is grown on top of Si waveguide and is designed with a vertical P-I-N structure. At 30C, the WGPD's typical dark current at -2.6V is less than 100nA. Fig. 3(a) shows the responsivity test result on a device measured at room temperature. The responsivity for both TE and TM modes are saturated at -1V. TE responsivity has a value of 0.75A/W, and TM responsivity has a value of 0.65A/W. High speed measurements with 50 Ohm RF termination showed a minimum bandwidth of 35GHz at bias of -1V. Ongoing process adjustment is expected to improve responsivity beyond 0.9A/W.

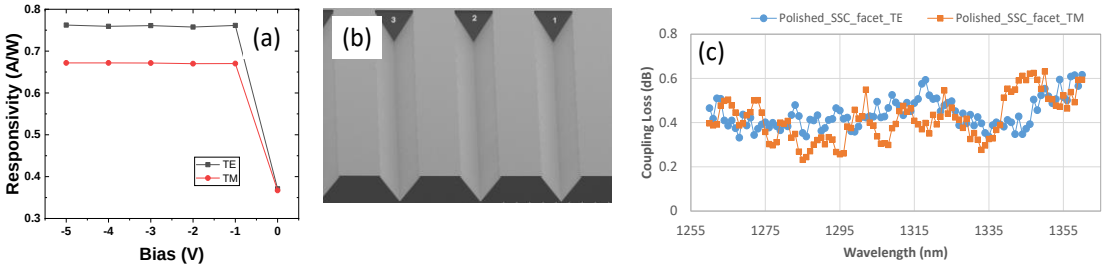

Fig. 3. (a) TE/TM mode Ge-PD Responsivity measured at room temperature, (b) Array of integrated V-grooves integrated with SiPIC, c) Plot of actively aligned coupling loss to SMF fiber vs wavelength of two different coupler facets (optimized for TE and TM respectively).

We have developed integrated V-groove arrays formed in front of an array of SSCs that allow for passive alignment to SMF28. Fig. 3(b) shows SEM images of processed V-grooves indicating smooth sidewalls achieved across an array. We measured coupling losses to a SMF from TE/TM SSC designs using active alignment. The best coupling achieved a mean coupling loss of ~0.5 dB for TE and TM polarizations at 1310 nm with up to 0.4 dB ripple over O-band, as shown in Fig. 3(c). The SSC facet was polished and AR coated prior to collecting these measurements. The simulated coupling loss when using active alignment was ~0.35 dB at 1310 nm. In comparison,

we collected data from SSC with facets that were processed lithographically along with V-grooves etched in the substrate. For two different V-groove widths, where one is 2 um wider relative to the other, the mean coupling losses were measured across multiple dies and channels to be close to 1.16 dB with good repeatability. Misalignment tolerance measurements performed using active fiber alignment show a ~0.3 dB penalty for +/- 1 um offset and the SSC facet roughness contributes ~0.4 dB loss. Accounting for this offset, the measured coupling losses using passive alignment and active alignment are nearly matched.

The 100Gbps PAM4 MRM we used in our integrated SiPIC has a 10um ring radius and is designed close to the critical coupling condition to achieve >20dB extinction ratio (ER) and free spectral range of 6.7nm. The process is similar to the device presented in [8]. The quality factor of such ring resonator is close to 5.5k to reduce the required driving swing voltage, while keeping the optical bandwidth over 40GHz. Fig. 4(b) shows the MRM resonance shift with reverse bias on the PN junction. 2V voltage DC swing around -2V results in 6dB ER, when ring is biased at 6dB IL. Average measured phase efficiency from these rings is 0.52 V.cm measured at -1.5V bias. Further we evaluated the high-speed performance of MRM. Fig. 4(b) and (c) show the transmitted eye diagram, where the ring diode was driven by 53 GBd PAM4 PRBS13 pattern, without and with pre-emphasis respectively. The ring was biased at -2V and driven using 2.5Vpp through a 50-Ohm terminated single ended RF probe. The optical waveform is analyzed using commercial DCA with SIRC filter enabled, per IEEE standard. The waveform measures TDECQ of 1.2 dB, extinction ratio of 4.6 dB, and level separation mismatch ratio of 0.96 with the use of pre-emphasis and TDECQ of 1.7 dB, extinction ratio of 5.3 dB without pre-emphasis.

In order to evaluate the fully integrated SiPIC performance with integrated lasers, a control loop was put in place using the integrated Ge-PDs in order to control the ring IL at close to 6dB. The SiPIC temperature was modulated while the control loop is active for over 10 minutes. Fig. 4(d) shows the relative modulation of temperature that was quantified to be ~8.5C, changing as fast as 45C/min by monitoring the laser wavelength. The post-FEC bit-error-rate was measured simultaneously with temperature modulation and shown in Fig. 4(e). Despite aggressive temperature modulation, the control loop maintains the proper state of the ring resulting in error-free operation of our integrated SiPIC including laser and MRM over the aggressive rate of temperature changes.

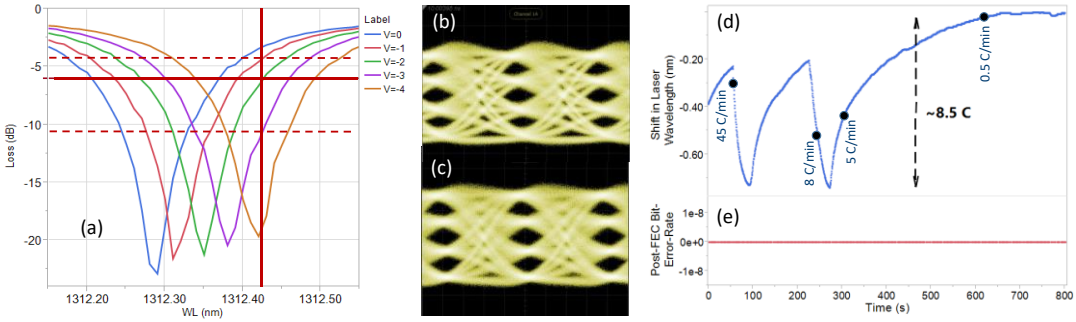

Fig. 4. (a) Transmission spectra resonance shift of MRM with applied bias, showing 6dB ER with 2V swing. Optical transmitted eye (b) without and (c) with pre-emphasis. (d) Laser wavelength shift during BER test, (e) post-FEC error rate over time.

3. Conclusion

In conclusion, we have designed, developed and demonstrated a 1.6Tbps silicon photonics integrated circuit with integrated lasers, MZ switches for laser redundancy, micro-ring modulator with integrated GePD monitors, 9um spot size converter with integrated V-grooves and high speed GePDs. The integrated device was tested using a control loop and 100Gbps PAM4 post-FEC error free operation was achieved with temperature ramp as high as 45C/min.

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