Micro-transfer-printed III-V-on-silicon distributed feedback lasers

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Abstract: We report on III-V-on-silicon DFB lasers realized by micro-transfer-printing pre-fabricated III-V semiconductor optical amplifiers on a silicon waveguide circuit comprising a first-order quarter wave shifted grating. Single mode operation at 1530 nm is demonstrated.

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1. Introduction

Wafer-scale integration of III-V semiconductors on silicon photonic integrated circuits is of key importance to realize fully integrated complex photonic systems-on-chip. Various approaches are currently being pursued to realize this (pick-and-place of micro-packaged lasers, flip-chip integration, die-to-wafer or wafer-to-wafer bonding, hetero-epitaxial growth), with different levels of maturity. A newcomer in the field of III-V-on-silicon photonic integrated circuits is micro-transfer-printing (μTP), illustrated in Fig. 1.

μTP combines advantages of flip-chip integration and wafer bonding. The process starts with the definition of the III-V devices (in this case semiconductor optical amplifiers) on a III-V source wafer (InP in our case), which has the active epitaxial layer stack grown on top of a release layer (InGaAs/InAlAs for the InP material system). After patterning of the device and the release layer, the structures are encapsulated and the release layer is selectively removed using $FeCl_3$:H_2O wet etching, leaving the III-V devices attached to the III-V substrate by thin tethers. With a polydimethylsiloxane (PDMS) stamp one or more thin-film III-V components can be picked up from the source wafer and printed onto a silicon photonic target wafer. The bonding of the SOA coupons to the silicon photonics target wafer can be realized using molecular bonding or using an adhesive bonding agent (used in this paper). Then, the encapsulation is removed on the target wafer and the III-V devices are electrically contacted on wafer level. This approach enables pretesting of the III-V devices on the source wafer, similar to flip-chip integration, but also massively parallel integration, similar to the die-to-wafer bonding approach. The III-V devices are micro-scale, so the silicon photonics back-end flow is not disturbed. Only a local opening to the silicon device layer is needed, similar to the flip-chip integration approach.

In this paper we demonstrate a III-V-on-silicon DFB laser by integrating a pre-processed III-V semiconductor optical amplifier using micro-transfer-printing on a quarter wave shifted distributed feedback cavity implemented in a silicon photonics waveguide circuit.

2. Design and fabrication of the III-V-on-Si DFB laser

The III-V epitaxial layer structure used to fabricate the SOAs is also illustrated in Fig. 1. The SOA epitaxial stack contains a 200 nm highly-doped p-InGaAs contact layer, a 1.5 μm p-InP cladding, a 25 nm InGaAsP etch stop layer, a pair of 40 nm AlInGaAs transition layers separating the InP cladding layers from the separate confinement heterostructure (SCH) layers, a pair of 75 nm AlGaInAs SCH layers, an active region with 6 AlInGaAs QWs sandwiched between AlInGaAs barriers (C-band gain spectrum), a 200 nm n-InP contact layer with 60 nm intrinsic InP layer underneath and a 50 nm/500 nm InGaAs/AlInAs release layer grown on the InP substrate.

A challenge in micro-transfer-printing pre-fabricated SOAs on top of silicon photonic circuits is the need of high alignment accuracy. State-of-the-art transfer printing tools provide an alignment accuracy of $\pm$1.5 μm (3σ). The micron-scale accuracy of the transfer printing tool requires good alignment tolerance of the adiabatic taper structure used to couple light from III-V to Si waveguide and vice versa [1]. Therefore, we use an alignment-tolerant adiabatic taper design discussed in detail in [2]. The alignment-tolerant adiabatic taper can provide alignment tolerance of 1.0 μm with a coupling loss less than 0.3 dB.

The silicon device layer is 400 nm thick and it is etched 180 nm to define the waveguides, shown in Fig. 2. The

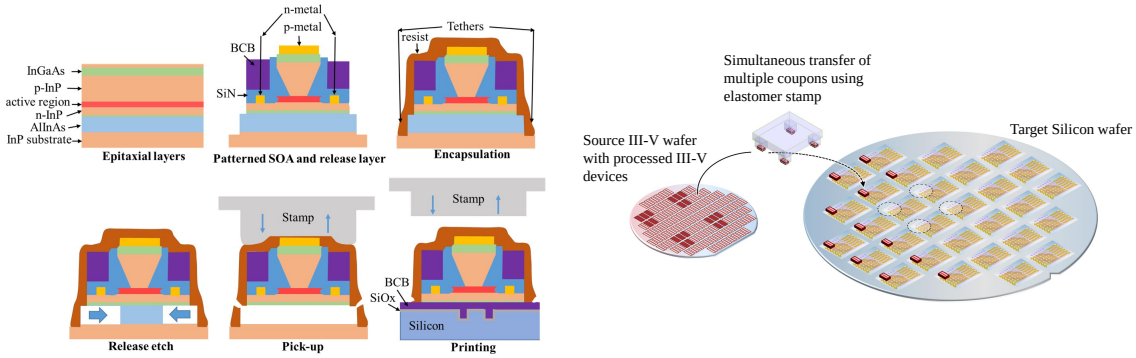

Fig. 1. (left) The micro-transfer printing process flow for SOA integration includes patterning of the device functional layers and release layer on the InP substrate, encapsulation of the device and the formation of the tethers to hold the devices in place during the release etch. Finally, the released devices are picked with an elastomer stamp and printed on the target site on the SOI wafer. (right) The concept of wafer-scale parallel printing of processed III-V devices on a target silicon photonics wafer using a multiple-post elastomer stamp.

DFB gratings are etched 30 nm on the surface of the waveguide. The buried oxide layer (BOX) is 2 μm thick underneath the silicon device layer. We use grating couplers to couple light out of the chip. The III-V SOA is 950 μm long including a 500 μm gain section and two 225 μm III-V alignment-tolerant adiabactic tapers on both sides of the SOA. The III-V waveguide width in the gain section is 3.2 μm and the DFB grating is 3.0 μm wide and 500 μm long, with a quarter wave shift in the middle. The grating has a period of 235 nm and a duty cycle of 0.6 (ratio between the etched slits and the period).

The III-V devices are pre-procesed in dense arrays on the source wafer , shown in Fig. 3(a), and then micro-transfer-printed on the SOI waveguide. The pre-processing steps include classical III-V processing steps, such as formation of the SOA mesa, metallization and n-InP patterning. What is specific about the devices for micro-transfer-printing is that below the SOA epitaxial layer stack a 50nm/500 nm thick InGaAs/InAlAs release layer is incorporated, that is patterned and encapsulated (using photoresist) together with the device, after which the release layer is selectively etched using $FeCl_3$:H_2O. The top view of the released devices is shown in Fig. 3(b). After release, the devices are micro-transfer-printed on the SOI photonic IC using a 20 nm thick DVS-BCB adhesive bonding agent. A top view of a micro-transfer-printed SOA is shown in Fig. 3(c). After the printing, the encapsulation is removed and the p-metal and n-metal are exposed and the devices are electrically connected, as shown in Fig. 3(d).

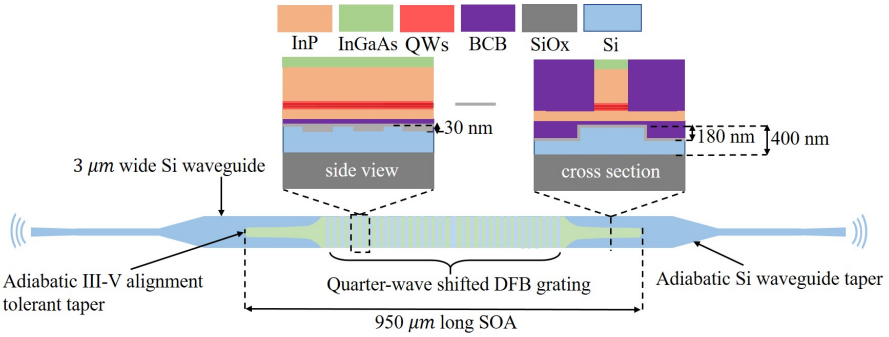

Fig. 2. Schematic illustrating the design of the III-V-on-Si SOA and the DFB grating. It also illustrates the cross-section drawing in the adiabatic taper and side view of the grating section of the device.

3. Device characterization

The III-V-on-silicon PIC is placed on a temperature-controlled stage for the measurements and kept at 20 ^{o}C. The PIC is optically probed with cleaved standard single mode fibers using a fiber stage. Grating couplers are used to interface with the optical fibers. The grating couplers that couple light out of the PIC have a wavelength dependent

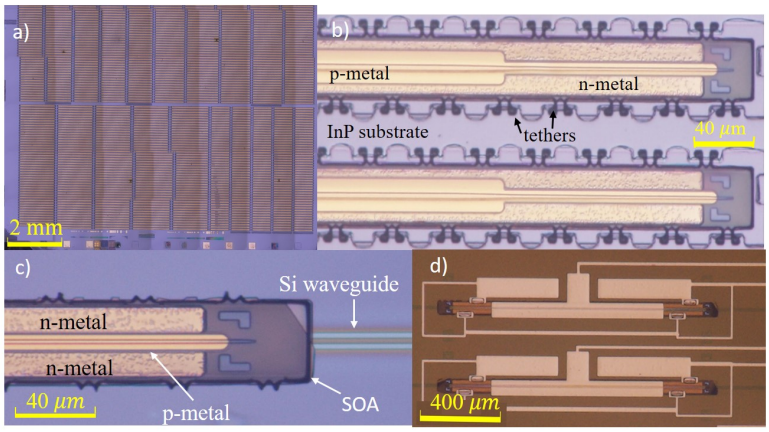

Fig. 3. a) The microscope top image of a dense array of SOA devices patterned and released on the native InP substrate, b) The zoomed-in top image of two SOA coupons, c) The SOA coupon after printing on the SOI waveguide, d) The microscope top image of two DFB lasers after the final metallization step on the target substrate.

transmission response. To calibrate out the grating coupler response, reference passive silicon waveguides are also fabricated on the III-V-on-silicon PIC and they undergo the same processing steps as the grating couplers used for interfacing with the DFB laser. The DFB laser is electrically probed with needles and is biased through a Keithley 2400 source meter. The series resistance of the laser is 8 Ω. Figure 4(a) shows the spectrum of the DFB laser for various bias currents. Single mode operation with a sidemode suppression better than 33 dB is obtained. The DFB tunes over 1.4 nm in wavelength when the bias current is varied from 60 mA to 140 mA. The single-sided laser ouput power at 130 mA is 3.75 mW. The threshold current of the laser is 62 mA.

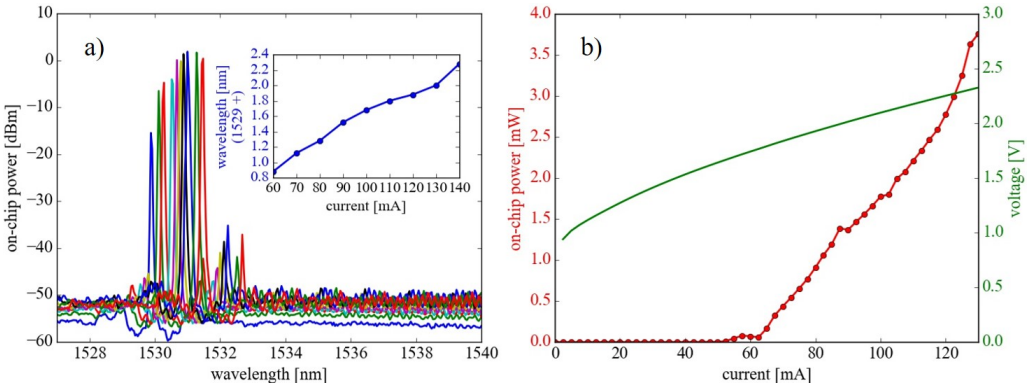

Fig. 4. a) The spectrum of the DFB laser with varying bias current. The inset shows the wavelength shift as a function of bias current. b) waveguide-coupled output power (single-sided) as a function of bias current and current-voltage characteristic

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