Heterogeneous Co-Integration of BTO/Si and III-V technology on a Silicon Photonics Platform

Pascal Stark¹, Felix Eltes¹, Yannick Baumgartner¹, Daniele Caimi¹, Youri Popoff^{1,2}, Norbert Meier¹, Lukas Czornomaz¹, Jean Fompeyrine¹, Bert Offrein¹, Stefan Abel¹

¹IBM Research – Zurich, Säumerstrasse 4, 8803 Rüschlikon, Switzerland ²Empa, Swiss Federal Laboratories for Materials Science and Technology, Überlandstrasse 129, 8600 Dübendorf, Switzerland crk@zurich.ibm.com

Abstract: We demonstrate for the first time the heterogeneous co-integration of Si photonics, BTO/Si for high-speed modulation and III-V materials for photodetection and emission. We show light coupling with losses <0.5 dB between the different functional layers. © 2020 The Author(s)

1. Introduction

Cost-efficient optical interconnects providing a high bandwidth and good power efficiency [1] are a key technology to cope with the ever-increasing traffic in data centers [2]. We extend the capabilities of the silicon photonics platform by heterogeneous integration of both, barium titanate (BTO)/Si technology as well as an ultra-thin, CMOS compatible III-V technology. Our BTO/Si technology offers record high Pockels coefficients [3], enabling the realization of power efficient, high-speed modulators (Fig. 1a) [4]. Fig. 1b shows an eye diagram of a 20 Gbps signal from a BTO modulator fabricated on a Si photonics platform. Efficient modulation at frequencies >65 GHz has already been demonstrated using different device designs [3]. The III-V technology enables high speed photodetection at 100 GBaud and beyond and offers a path towards light emission [5–7]. Fig. 1e shows the frequency response as well as an eye diagram of a III-V based photodetector (PD) integrated on silicon photonics, operating at 32 Gbps. The heterogeneous integration scheme (Fig. 1c) offers a path towards high bandwidth, power efficient and compact optical transceivers. Beyond optical networking, co-integrating these technologies could be an enabling factor for photonic signal processing by bringing in new functionality to the Si photonics platform, e.g. non-volatile optical weights based on BTO/Si or III-V based semiconductor optical amplifiers, both of which can serve as crucial building blocks for optical neural networks [8].

Si photonics, BTO/Si and III-V technology are fabricated using different processing techniques involving molecular beam epitaxy and MOCVD, which are not directly compatible with each other. In this paper we show for the first time the heterogeneous co-integration of Si photonics, BTO/Si and III-V technology on a single wafer. We illustrate how light can be transferred between the layers using an adiabatic coupling scheme. We demonstrator how to co-integrate these three functional layers and we show light coupling with losses <0.5 dB between the layers.





integrated on a Si wafer. (e) Frequency response of photodetector. Inset: Eye diagram at 32 Gbps (NRZ) without using digital signal processing. 2. Integration and Light Coupling Concept

Here we co-integrate Si photonic devices (220nm Si on 2µm buried oxide) with a BTO/Si stack (100nm BTO) and an intrinsic InP layer (250nm) (Fig. 1c). As the integration process is similar for active and passive devices, we use passive devices to demonstrate the co-integration and coupling. The separate integration of active BTO and III-V based active devices on a Si photonics platform was demonstrated previously [4,5]. Instead of using a quantum well III-V material stack, we choose an intrinsic, low-loss InP layer, which serves as seed layers for subsequent re-growth steps for active devices [5].

T3B.4.pdf

We start the integration by fabricating Si photonic structures on a silicon-on-insulator (SOI) substrate (host wafer), followed by deposition of a SiO₂ cladding layer. The cladding is then planarized by chemical mechanical polishing (CMP). BTO thin films are epitaxially deposited on a SOI substrate and transferred onto the SOI host wafer using molecular wafer bonding. After bonding the BTO wafer, its substrate is removed from the backside and hybrid BTO/Si waveguides are processed. Another SiO₂ cladding an epitaxially grown InP layer to the Si, BTO/Si stack. Subsequently, InP waveguides are processed. The cross sections in Fig. 2a-c visualize the successful co-integration of the different materials with separate Si, BTO/Si and InP waveguides on different layers.

Light is transferred between the layers using two tapers with inverse direction (Fig. 2d). Light is for example coupled from a Si to a BTO/Si waveguide by slowly reducing (taper down) the Si waveguide and at the same time increasing the BTO/Si waveguide width (taper up). By reducing the Si waveguide width its mode index decreases, vice-versa increasing the BTO/Si taper width leads to an increase of the index. The optical mode will propagate towards the region, where its effective index is the highest. Therefore, the mode moves from the Si waveguide to a hybrid mode and is finally transferred completely to the BTO/Si waveguide (Fig. 3a-c).



Fig. 2 (a) Focused Ion Beam (FIB) cross section showing two InP, a BTO/Si and a Si waveguide. (b) Schematic of the waveguides shown in the FIB cross section (a). (c) FIB cross section in coupler region (Si ↔ BTO/Si), showing a small offset in the lateral alignment.
(d) Tapers are used to efficiently transfer guided light between the different layers.

3. Coupling Experiments

In our experiments we extracted the coupling loss between the layers using linear tapers. A mask with a varying number of coupler pairs but constant propagation length was designed. The coupling efficiency was characterized separately between Si \leftrightarrow BTO/Si and BTO/Si \leftrightarrow InP waveguides for linear tapers of different lengths (Fig. 3e, inset). As expected, the coupling loss between the layers scales linearly with the number of coupler pairs in the link (Fig. 3e). We achieved coupling losses of 0.48 dB (Si \leftrightarrow BTO/Si) and 0.34 dB (BTO/Si \leftrightarrow InP, measured without InP cladding), respectively. The waveguide propagation losses are 7.8 dB/cm (Si), 7.5 dB/cm (BTO/Si) and 6.0 dB/cm (InP). These propagation losses were limited by the fabrication in our research cleanroom environment, using optimized processes losses below 3 dB/cm can be reached for all three material systems.

Fig. 3f shows a normalized transmission spectrum measured after coupling light through all three layers, from Si to BTO/Si to InP and back. The adiabatic couplers work over a broad wavelength range, in this experiment the bandwidth was limited by the grating couplers used to couple light in and out of the chip.

4. Taper Optimization

Using linear tapers the coupling losses were <0.5 dB, which is feasible in applications where light is coupled only few times between the layers. In the following we discuss how the taper shape can be optimized to further reduce the coupling losses for applications where the power budget is low (e.g. optical transceivers), or light is transferred many times between the layers (optical neural networks). Two loss mechanisms contribute to the coupling loss of the light transfer between the layers: mode transfer loss and propagation loss caused by sidewall roughness. To keep the mode transfer loss low, long, adiabatic tapers are required. On the other hand, shorter tapers have lower propagation loss. A good tradeoff is to implement the shortest possible adiabatic taper. In our experiments the loss was decreasing with increasing taper length, indicating that the mode transfer loss dominated over the propagation loss for all tested taper lengths. To optimize the taper shape, we simulated the waveguide modes in multiple cross sections along the taper and calculated the mode overlap between consecutive layers (Fig. 3a, c). To keep the total losses low, the taper slope

T3B.4.pdf



Figure 3 (a) The fundamental modes were simulated at different cross sections along a Si \leftrightarrow BTO/Si coupler ($|E|^2$). (b) Field profile ($|E|^2$) along the coupler ($|z|^2$).

the coupler (y-z cut). (c) Mode overlap between modes at different, consecutive cross sections along the taper. (d) Simulated transmission for linear and optimized tapers of different lengths (Si ↔ BTO/Si). Inset: Shape of optimized taper (three linear segments). (e) Transmission as a function of the number of coupler pairs for linear tapers of different lengths. Inset: Coupling loss per coupler (BTO/Si ↔ InP) as a function of the taper length. (f) Normalized transmission spectrum after coupling light through all three layers and back. Inset: Schematic of measurement setup. should be low in sections where the mode overlap is small and can be high where the overlap is large. In a first order approximation we designed tapers that consist of three linear segments with varying slope (Fig. 3d, inset). We implemented such a taper model in Lumerical Mode (eigenmode expansion solver) and computed the mode transfer efficiency for tapers of different lengths (Fig. 3d). The model does not include propagation loss, hence the coupling efficiency remains close to 100% after reaching the taper length required for adiabatic coupling. We find that linear tapers of 500µm length and optimized tapers (three linear segments) of 86µm length show mode transmission >99.5%. Assuming the propagation loss in the optimized and the linear tapers are equal, we find that the total coupling loss using the optimized tapers is approximately 6 times smaller than for linear tapers.

5. Conclusion

In this paper we demonstrated for the first time the co-integration of Si photonics, BTO/Si and III-V technology. Light is transferred between the layers with coupling losses <0.5 dB and we discussed how the coupling loss can be further reduced by optimizing the taper shape. The co-integrated technologies offer exciting physical effects like a strong Pockels effect (BTO/Si) and optical gain/emission (III-V), and extend the capabilities of the versatile Si photonics platform. This technology paves not only the way for high bandwidth, power efficient and compact optical transceivers but enables novel photonic devices and systems, as for example optical neural networks.

6. Acknowledgments

This project has received funding from the EU-H2020 research and innovation program under grants no. 688003 (DIMENSION), 688579 (PHRESCO) and 780997 (plaCMOS).

7. References

- 1. L. Pavesi and D. J. Lockwood, eds., Silicon Photonics III, Topics in Applied Physics (Springer Berlin Heidelberg, 2016), Vol. 122.
- 2. "Cisco Global Cloud Index: Forecast and Methodology, 2015-2020," White Pap. (2016).
- S. Abel, F. Eltes, J. E. Ortmann, A. Messner, P. Castera, T. Wagner, D. Urbonas, A. Rosa, A. M. Gutierrez, D. Tulli, P. Ma, B. Baeuerle, A. Josten, W. Heni, D. Caimi, L. Czornomaz, A. A. Demkov, J. Leuthold, P. Sanchis, and J. Fompeyrine, "Large Pockels effect in micro- and nanostructured barium titanate integrated on silicon," Nat. Mater. 18, (2019).
- F. Eltes, C. Mai, D. Caimi, M. Kroh, Y. Popoff, G. Winzer, D. Petousi, S. Lischke, J. Elliott Ortmann, L. Czornomaz, L. Zimmermann, J. Fompeyrine, and S. Abel, "A BaTiO3-Based Electro-Optic Pockels Modulator Monolithically Integrated on an Advanced Silicon Photonics Platform," J. Light. Technol. 37, 1456–1462 (2019).
- Y. Baumgartner, M. Seifried, C. Caer, P. Stark, D. Caimi, J. Faist, B. J. Offrein, and L. Czornomaz, "Novel CMOS-Compatible Ultralow Capacitance Hybrid III-V/Si Photodetectors Tested up to 32 Gbps NRZ," in *Optical Fiber Communication Conference (OFC)* 2019 (OSA, 2019), p. Th3B.3.
- M. Seifried, G. Villares, Y. Baumgartner, H. Hahn, M. Halter, F. Horst, D. Caimi, C. Caer, M. Sousa, R. F. Dangel, L. Czornomaz, and B. J. Offrein, "Monolithically integrated CMOS-compatible III-V on silicon lasers," IEEE J. Sel. Top. Quantum Electron. 24, (2018).
- K. Takeda, T. Sato, A. Shinya, K. Nozaki, W. Kobayashi, H. Taniyama, M. Notomi, K. Hasebe, T. Kakitsuka, and S. Matsuo, "FewfJ/bit data transmissions using directly modulated lambda-scale embedded active region photonic-crystal lasers," Nat. Photonics 7, 569–575 (2013).
- S. Abel, F. Horst, P. Stark, R. Dangel, F. Eltes, Y. Baumgartner, J. Fompeyrine, and B. J. Offrein, "Silicon photonics integration technologies for future computing systems," in 2019 24th OptoElectronics and Communications Conference (OECC) and 2019 International Conference on Photonics in Switching and Computing (PSC) (IEEE, 2019), pp. 1–3.