1.6Tbps Coherent 2-Channel Transceiver Using a Monolithic Tx/Rx InP PIC and Single SiGe ASIC

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Abstract: We present a 1.6Tbps coherent transceiver delivering 800Gbps/wave transmission using integrated Tx/Rx functions with 50GHz bandwidth and 50kHz linewidth tunable lasers on a single 2-channel InP PIC, paired with a SiGe Driver and TIA ASIC.
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1. Introduction

Over the last two decades, the commercial development of multi-channel photonic integrated circuits (PICs) for transmitter and receiver solutions has resulted in significant benefits to the economics, power consumption, density, and reliability of high capacity DWDM systems [1,2]. While high performance multi-channel InP PICs have managed to incorporate a large number of functions onto a single chip, including both active and passive components, they have historically continued to use separate PICs for transmitter and receiver functions. Silicon photonic devices, on the other hand, have managed to co-integrate transmitter and receiver functions [3] albeit without integrated on-chip lasers and amplifiers needed to realize a complete monolithic solution.

In the past, we have reported on separate InP Rx and Tx PICs capable of 88-100Gbaud transmission [4-6]. In this paper, we report on the development of a fully monolithic coherent 2-channel InP-based PIC that integrates all of the requisite functions for two full transmitter and receiver channels onto a single PIC. These functions include high performance I/Q modulators, coherent receivers, on-chip narrow linewidth widely tunable lasers and semiconductor optical amplifiers (SOAs). A matching monolithic SiGe high performance 2-channel ASIC is also reported here that integrates two channels of MZM drivers and TIAs capable of over 50GHz bandwidth, sufficient for high performance at upto 100GBaud data rates. Each of the components in the integration platform deliver industry-leading performance, demonstrated by the capability to achieve 800Gbps/wave transmission in 95GHz wide channels over the C-band, and will enable the realization of future generations of optical engines.

2. InP PIC and SiGe ASIC Architecture

Figure 1a shows a schematic of the coherent transceiver PIC and ASICs. The InP PIC integrates two full coherent

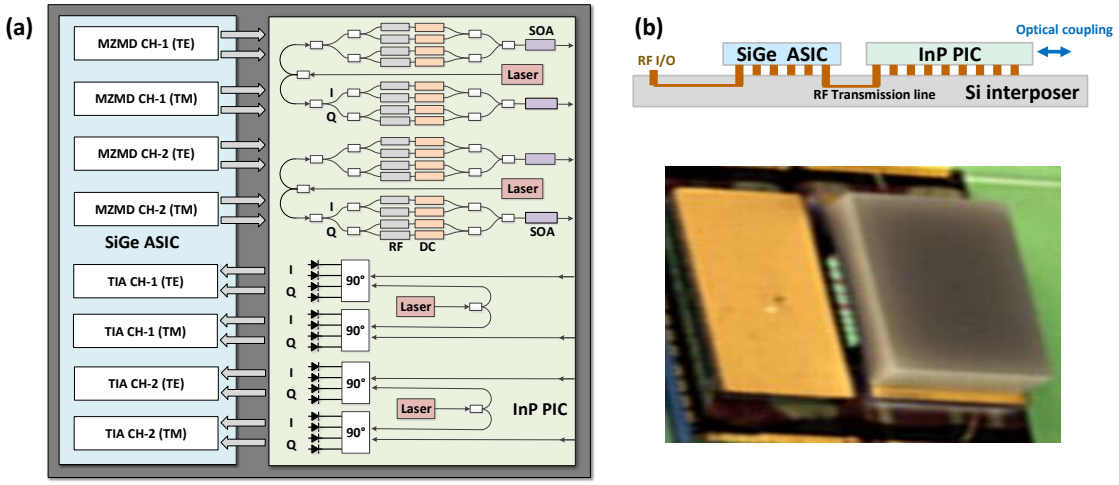

Figure 1. a) Schematic of coherent 2-channel transceiver with single-chip Tx/Rx InP PIC and matching SiGe single-chip MZMD/TIA ASIC. b) Cross-section schematic and optical image of the PIC+ASIC flip-chip subassembly.

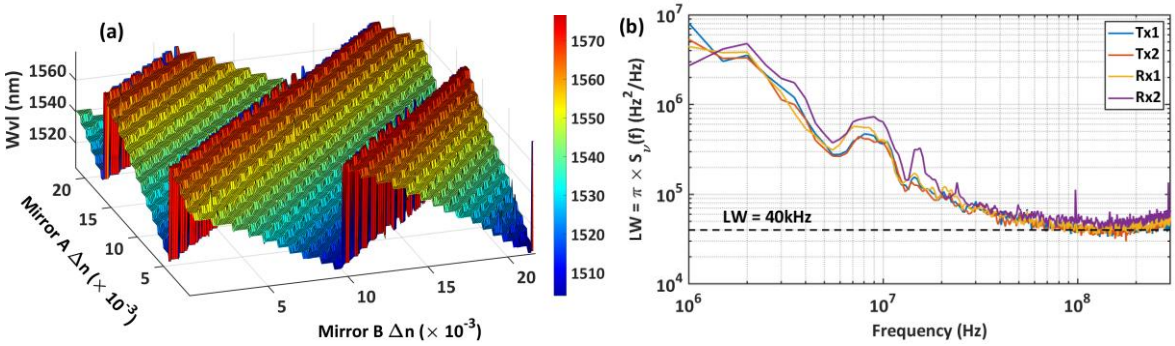

Figure 2. a) Typical tuning map of an on-chip tunable laser source showing extended C-band coverage. b) PSD spectra of all 4 tunable laser sources on a single PIC showing 40-60 kHz cavity linewidth.

transmitter channels and two full coherent receiver channels onto a single chip. Each transmitter channel consists of an extended C-band tunable laser that feeds into a pair of nested I/Q modulators, one for each polarization state, designed to operate at a Vπ of 1.9V. An on-chip SOA amplifies the output of the modulator prior to being routed to the optical facet to ensure high output power and high launch OSNR. Each receiver channel on the PIC also integrates a dedicated tunable laser that feeds into a 90-degree optical hybrid, coupled to a pair of balanced high-speed photodiodes. The integrated tunable lasers supplying the receiver channels include a power tap that is routed to the facet for test and calibration purposes. Separate tunable lasers allow completely independent tuning of the Tx/Rx channels on the PIC, enabling greater network reconfigurability than a single shared Tx/Rx laser per channel typically implemented in silicon photonics transceiver solutions [3].

The matching SiGe transceiver ASIC shown in Fig. 1a is fabricated in a 180 nm BiCMOS process. The Mach-Zehnder modulator driver (MZMD) consists of a 2-stage amplifier design featuring inbuilt equalization stages to provide a broadband linear gain. The transimpedance amplifier (TIA) circuit is designed with three stages and includes automated gain control (AGC) amplifiers and inbuilt equalization. The ASIC chip in total integrates 8 MZMD streams and 8 TIA streams onto a single die. The PIC and ASIC die are co-assembled in a hybrid integration process that flip-chip bonds them onto a common Si-interposer, shown in Fig. 1b, without needing wirebonds [4].

The on-chip lasers are capable of continuous tuning over the extended C-band of 4.8 THz [2] as shown by the laser wavelength tuning map as a function of the mirror refractive index change in Fig. 2a. The phase noise power spectral density (PSD) measurements [2] for each of the 4 (Tx+Rx) lasers on a PIC shows uniform performance across the C-band, corresponding to a linewidth of ~50 kHz as shown in Fig. 2b. Figure 3 shows a typical S21 response for the transmitter and receiver subassemblies demonstrating an analog bandwidth of more than 50 GHz. Electrical tests do not indicate a measurable crosstalk between neighboring MZMD and TIA streams in ASIC and indicate good isolation between Rx and Tx channels. The PIC and ASIC devices fabricated in our transceiver platform show similar performance as their counterparts fabricated in separate Tx/Rx device platforms [4-6] and demonstrate co-integration of Tx and Rx functions onto a single chip transceiver PIC without a performance penalty.

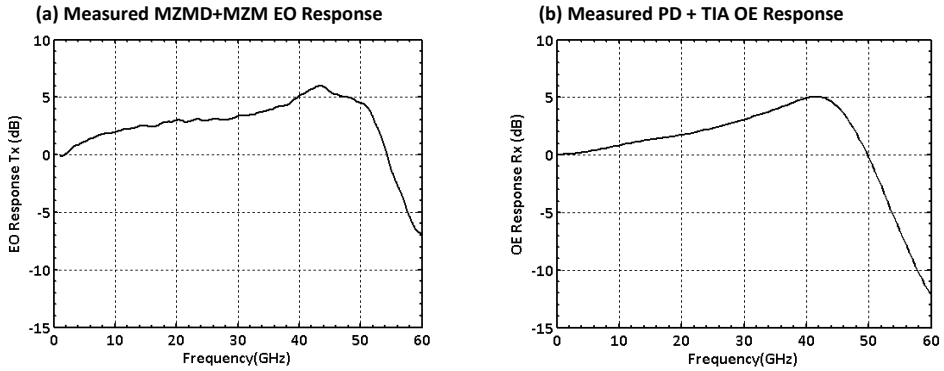

Figure 3. Overall small-signal RF frequency response of the PIC+ASIC flip-chip subassembly, demonstrating the bandwidth of the (a) transmitter (MZM+MZMD) and (b) receiver (PD+TIA) components.

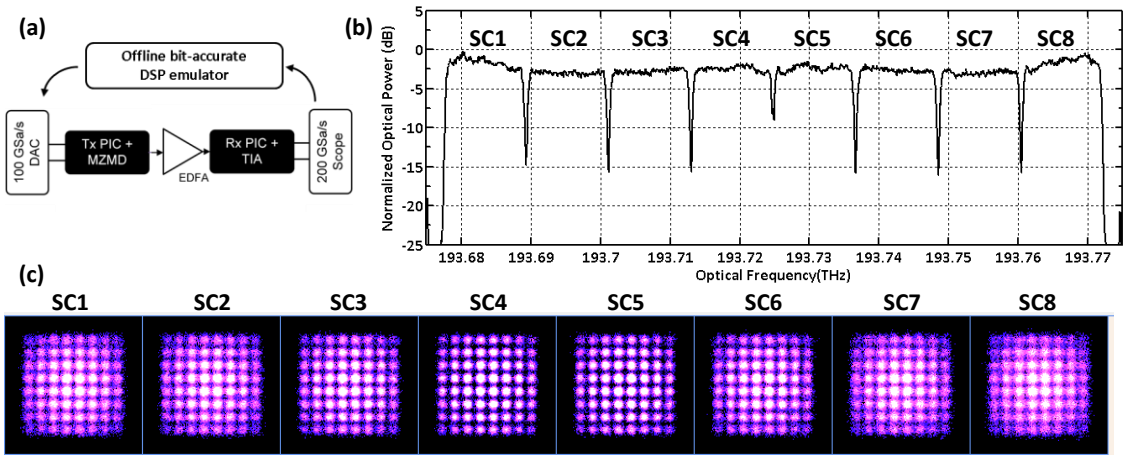

Figure 4. a) Experimental setup for 800Gbps transmission measurements. b) Transmitter optical spectra showing a single ~95GHz wide channel with 8 digital subcarriers (SC1-8). c) All received 8 subcarrier 64QAM constellations for a single polarization. Each subcarrier supports a 100Gbps payload for a total capacity of 800Gbps per wave.

3. Experimental 800Gbps/wave operation

The PIC and ASIC transceiver sub-assemblies were characterized for 800Gbps transmission. A 100GSa/s DAC was used to generate the transmission signal that was fed to the interposer via RF cables and a microwave probe. The output optical signal was then coupled to a receiver channel, and the output of the TIA was connected to a set of real-time scopes operating at 200GSa/s. Due to probing limitations in the setup, the characterization was done on a single polarization at a time.

The 800Gbps/wave transmission in this paper was accomplished using a 90GBaud data stream, comprised of 8 digital Nyquist subcarriers [7,8] resulting in a ~95GHz wide channel. Each subcarrier supports a probabilistic constellation shaped (PCS) 64QAM data stream [9] with a data payload of 100Gbps, for a total capacity of 800Gbps per wavelength. The signal processing at the receiver was done using an offline bit-accurate DSP emulator that includes FEC gain sharing, chromatic dispersion compensation and linear equalization blocks, but refrains from using non-linear optimization. Overall Q^2 of the received signal, estimated from the pre-FEC BER [4], was measured to be >7.5dB under back-to-back conditions, demonstrating sufficient margin for transmission over a real network.

4. Conclusion

We have demonstrated a 1.6Tbps coherent 2-channel transceiver comprised of a monolithic Tx/Rx InP PIC, with integrated narrow linewidth C-band tunable lasers and on-chip SOAs, and a monolithic 2-channel SiGe MZMD and TIA ASIC. The two chips were flip-chip bonded onto a Si-interposer to form a compact PIC/ASIC subassembly capable of 50GHz bandwidth, sufficient for 90-100GBaud data rates and the realization of 800Gbps/wave transmission. This experiment demonstrates the next step in the evolution of highly integrated transceivers to continue to reduce cost and size, and to provide increased bandwidth and uncompromised performance for next generation optical engines.

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