Electrical and Optical Reliability Analysis of GeSi Electro-Absorption Modulators

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Abstract: Reliability analysis on Electro-Absorption Modulators reveals two degradation parts, trap generation and filling of pre-existing defects on Ge/Si and Ge/Ox interface. After stress, electro-optical extracted parameters indicate no impact of temperature, bias or stress time.

OCIS codes: (230.4110) Modulators, (200.4650) Optical interconnects

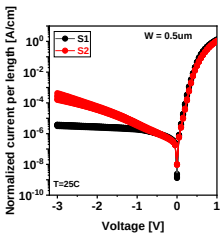
1. Introduction

Over the past several years, Silicon Photonics has emerged as a key photonic integration platform targeting next-generation optical interconnects [1, 2]. One of the main building blocks of this technology is the GeSi Electro-Absorption Modulator (EAM). These devices exploit the Franz-Keldysh (FK) effect in epitaxially grown GeSi or Ge, to enable high-speed modulation in a compact footprint and with low dynamic power consumption [3]. In order to use these devices in actual applications, they need to pass stringent reliability criteria [4-5]. In this work, we extend our analysis to GeSi-based EAMs, aiming to understand the relevant device degradation mechanism and to predict the EAM device lifetimes under typical application scenario's and failure criteria.

2. Devices and experiments

A. Device description

The GeSi EAMs studied in this work are lateral p-i-n diodes, with p-type and n-type ion implants both in Ge and Si and are fabricated in imec's 200mm Si Photonics platform [6-7]. Two EAM device designs, S1 and S2, both operating at a 1550nm, were tested in this work, and have a width of 0.5um and device lengths of 49.6um and 81.6um respectively, with S2 having a 30% higher Si content than S1. Fig. 1a-b shows the schematic cross-section of the structure and the normalized IV characteristics for both lengths. The values indicate that it is not the length that affects the higher leakage current, but the increased Si content. The same GeSi device structures can also be used as an efficient waveguide photodetector at the same wavelength by applying the appropriate bias voltage [8]. In our case, being used as a modulator, the operating (reverse) diode voltages are assumed to be in the range 0V-2V. Standard reliability tests were used; accelerated ageing over a wide range of temperatures and (un) biased Damp Heat. All the details of the conducted experiments are also shown in Fig. 1c.



Structures	Measurements	Temperature [C]	Stress bias [V]
S1/ S2	Acc. Ageing	125 - 150 - 175 - 200	-2
S1	Acc. Ageing	200	-5
S1/S2	Biased Damp Heat	85C/85%	-2
S1	Unbiased Damp Heat	85C/85%	0

Figure 1. (a) Cross-section of the EAM, (b) Wafer-level initial IVs showing the dark current difference for the two lengths and (c) Overview of the applied tests on each geometry

B. Experimental details

The first part of the experimental work is about the degradation mechanisms induced by electrical stress. Initial wafer-level electro-optical measurements were performed on the aforementioned structures, at room temperature in order to assess the devices' characteristics and use the extracted values as a comparison for the after-stress tests. The next step was dicing and bonding the samples on ceramic packages in order to start the stress sequence. As described before the used techniques are the Acc. Ageing and the (un) biased Damp Heat, both of them applied for >1000h at a constant bias. In addition, the ageing was interrupted between the stress loops to measure the dark current at the -2V bias, but this time at 85C. The details of the measurement sequence can be found in [4]. An average of 5 samples per condition was stressed in order to ensure the necessary statistics and conclude in safe

results. For the second experimental part, different batches of samples were taken out from all the above temperatures after various stress times, in order to be re-measured electro-optically, at room temperature again, and investigate the impact of stress time on the parameters of the devices.

3. Results and discussion

A. Stress results

Starting with structure S1, we calculate the dark current shift, in particular the difference of the measured I_{dark} in the intermediate measurements at 85C and the initial values. Plotting the data w.r.t. stress time for all stress temperatures, will help us determine the lifetime of our devices at 85C and -2V operating conditions. Since the damp heat test is taking place in the data treatment temperature, we will not report these values. Looking at Fig. 2a, it is clear that the degradation happens in two phases. For the lowest temperatures, hence the lowest dark current, we observe an incubation time that is followed by a power-law increase. However, as we move on to higher stress temperatures as well as higher bias voltage, the incubation time ceases to exist and a power-law dependence is dominating the degradation. Similarly to [5], the incubation phase can be considered to represent the filling of pre-existing defects while the leakage current increase (power-law part) is describing the creation of new traps. Following the same data treatment for structure S2 (Fig. 2b) we can see that there is no big variation between the tested temperatures. This is due to the fact that we start from a much higher leakage current, as it is already obvious from the room temperature results in Fig. 1b. So, the incubation time is no more 'active' and we have a direct power-law dependence which means a defect generation process. Simulating the electric field distribution at the same bias condition (-2V) can give us an indication of the position of the defect generation that appears to be at the Ge/Si interface and the Ge/Ox interface, that experience the highest e-field values.

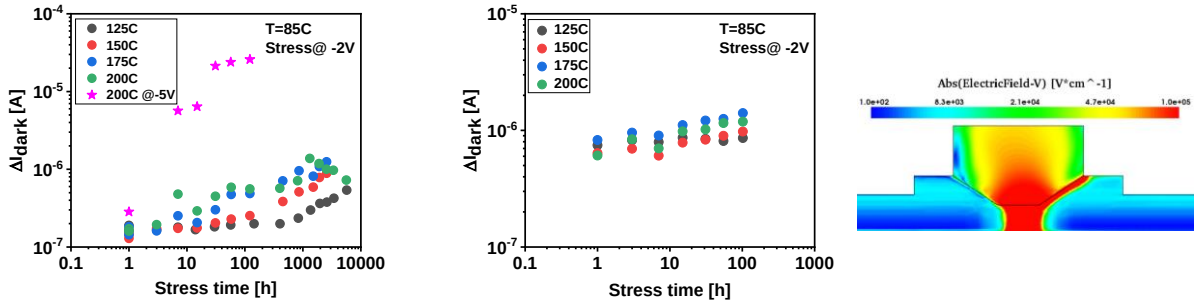


Figure 2. (a) Dark current shift at 85C for all tested temperatures shows that there is a two-phase degradation, incubation time and power-law dependence for S1 device, (b) ΔI_{dark} at 85C for S2 structure, (c) The defect generation occurs at the Ge/Si and Ge/Ox interface where the electric field simulation has the highest values.

Calculating, also, the power-law slopes for both dimensions, we see that for S1 values in the range of 0.23-0.45 are extracted with a decreasing temperature. On the contrary, the slopes from S2 are around 0.1 which would give too pessimistic predictions regarding the lifetime. Using the values from Fig. 2a, we plot the distributions in relation to the failure time and extract the lifetime predictions for a failure criterion of a 10x increase of the dark current for S1 (Fig. 3). From the fit, it is clear that the highest temperatures and the more aggressive applied voltage do not follow an Arrhenius behavior, an indicative of the defect generation that takes place in these conditions. Fitting the lowest temperatures, we extract the lifetime for two different temperatures and two percentiles as well as for two different criteria (Table II). Even at the more extreme requirements, the devices easily above the 10y lifetime.

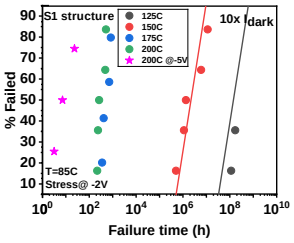


Figure 3. Failure distributions for S1, able to fit only the lowest applied temperatures

Table II. Lifetime extrapolation for S1

1uA crit	85C		125C	
Stress bias	0.1%	0.005%	0.1%	0.005%
-2V	6.04E+04y	2.33E+04y	27.7y	10.7y

$10xI_{dark}$ crit	85C		125C	
Stress bias	0.1%	0.005%	0.1%	0.005%
-2V	2.15E+06y	9.88E+05y	809y	372y

B. Electro-optical results

As mentioned before, different batches of samples were interrupted during the environmental tests and measured again optically at room temperature. For this part, we will only show the results of S1 structure. Figure 4 shows the

extracted electrical values of the diode ideality factor and the series resistance. Both parameters, regardless of the stress conditions, show no or minor variation after stress which proves the good quality of the diode.

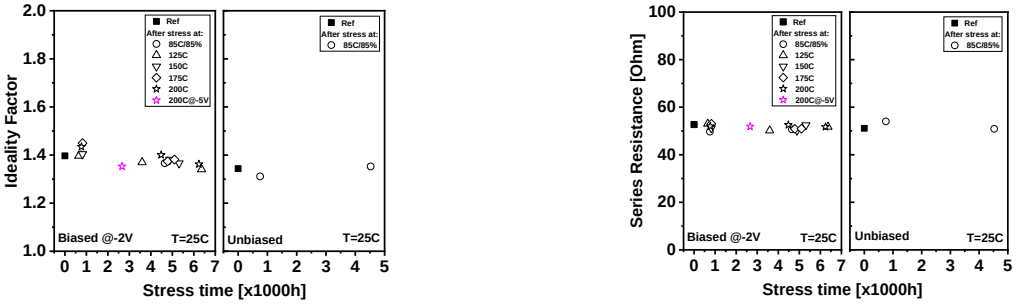


Figure 4. Extracted electrical diode parameters for all the tested temperatures, at biased and unbiased conditions (a) ideality factor appears unaffected from all the applied conditions, with a value of 1.4 for all the samples, (b) Similarly the series resistance of the diode remains around 50Ohm for almost 7000h of stress time.

At the same time, regarding the optical parameters, calculating the Extinction Ratio (ER) and the wavelength of maximum extinction ratio (ER) at 2Vpp, we observe no type of degradation for both parameters (Fig. 5). The extinction ratio remains around 4dB while the operating modulation wavelength of the device stays at its nominal value of 1550nm (C-band operation).

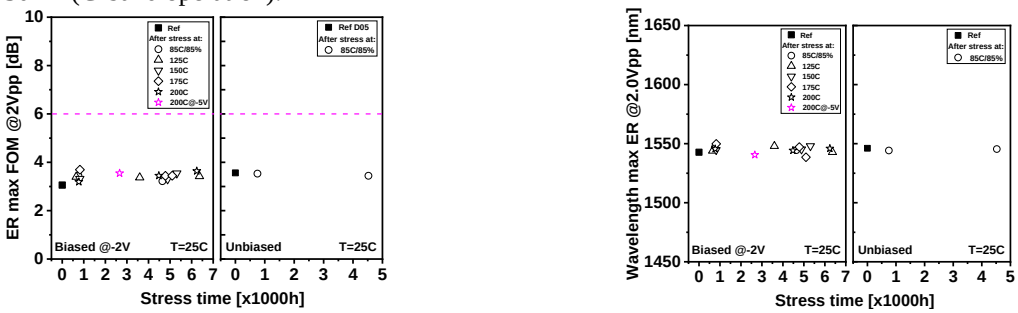


Figure 5. Extracted optical parameters for all the tested temperatures, at biased and unbiased conditions (a), the Extinction Ratio of the stressed samples remain on the same level as the reference ones and (b) the wavelength of the modulators at the maximum ER at 2Vpp is not modified after electrical stress.

4. Conclusions

We performed a detailed reliability study of GeSi Electro-Absorption Modulators integrated in a silicon photonics platform using a wide range of stress and performance parameters. Depending on the applied stress conditions, different mechanisms, such as filling of traps and/or creation of new ones, lead to an increase in dark current at -2V, where the dark current at -1V remained constant. At -2V, actual failures in the form of excessive dark currents are not expected to happen at normal operation conditions and times. Extending the study to electro-optical measurements has shown that temperature (up to 200°C), stress time (up to 5000h), humidity (up to 85% relative humidity at 85°C) are not affecting the extracted parameters of the EAMs. For the electrical part, besides the reported increase in dark current, the ideality factor and the series resistance remain unimpacted. Also the extinction ratio and the wavelength at 2Vpp remain unchanged after our reliability stresses.

Acknowledgments

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