16-Channel Membrane Directly Modulated Laser Array on Si for 2-km Transmission of 112-Gbps PAM-4

Takuro Fujii, Koji Takeda, Yoshiho Maeda, Nikolaos-Panteleimon Diamantopoulos, Tomonari Sato, Hiroki Sugiyama, Tai Tsuchizawa, Toru Segawa, and Shinji Matsuo

NTT Device Technology Labs, NTT Corporation, 3-1 Morinosato-Wakamiya, Atsugi, Kanagawa 243-0198 Japan, takuro.fujii@ntt.com

Abstract *Sixteen-channel DML array integrated with spot-size converters are fabricated on a SiO_2/Si substrate with a footprint of 1.11 × 2.75 mm^2, demonstrating 28- and 56-GBaud PAM4 operations and BERs below the KP4-FEC limit after 2-km transmission. ©2023 The Author(s)*

Introduction

The rapid growth of datacentre traffic has created a strong demand for optical transmitters with a small footprint, low power consumption, and low cost. A directly modulated laser (DML) is a strong candidate to meet these requirements. In addition, a photonic integrated circuit (PIC) containing many devices is important for reducing assembly cost. In this context, we have so far developed heterogeneously integrated III-V lasers with a membrane structure on a Si wafer with an intermediate SiO_2 layer [1], [2]. A membrane InP-based structure sandwiched between low-refractive-index silica layers provides a high optical confinement factor in the active region, which results in high modulation efficiency and low power consumption. The laser is connected to a spot-size converter (SSC) consisting of an inverse-tapered InP waveguide and SiO_x waveguide, which enables us to use butt coupling to the high-numerical aperture fibre (HNAF) [3].

Recently, we developed a 16-ch membrane DML array to increase the bandwidth density of the transmitter chip, i.e., total bit rate divided by the length of the chip facet. A direct modulation with a 32-Gbps non-return-to-zero (NRZ) signal was demonstrated for all 16 DMLs [4]. In this paper, we present a development of a new 16-ch DML array with the same layout but using a non-alloy contact instead of an alloy electrode, resulting in improved uniformity and differential resistance. We achieved 2-km transmission of 28- and 56-GBaud 4-level pulse amplitude (PAM-4) modulation using this newly developed DML array. Thanks to the integration of SSCs and low-loss SiO_x waveguides, fibre-coupled optical output power of > 1.6 mW was achieved with an average loss of −1.74 dB including SSC, SiO_x waveguide, and fibre-coupling. All 16-ch DMLs exhibited a bit-error rate (BER) below the KP-4 forward error correction (FEC) limit [5] after 2-km transmission without using an optical amplifier.

Device structure

Figure 1 (a) shows a schematic drawing of the 16-ch DMLs arrayed in 4 x 4 on a single chip. Each DML is integrated with an SSC, and optical outputs are obtained from the 1.11-mm-wide chip facet through the SiO_x waveguides. Figure 1 (b) shows a cross-sectional view of one of the DMLs. A 340-nm-thick III-V layer that includes 6-period InGaAlAs multi-quantum wells (MQWs) was originally grown on an InP substrate, and subsequently bonded to Si substrate with an intermediate SiO_2 layer. After the bonding, a buried-heterostructure was formed by carrying out epitaxial regrowth of an undoped InP layer. The p-type doping was carried out by the thermal diffusion of Zn, and n-type doping was carried out

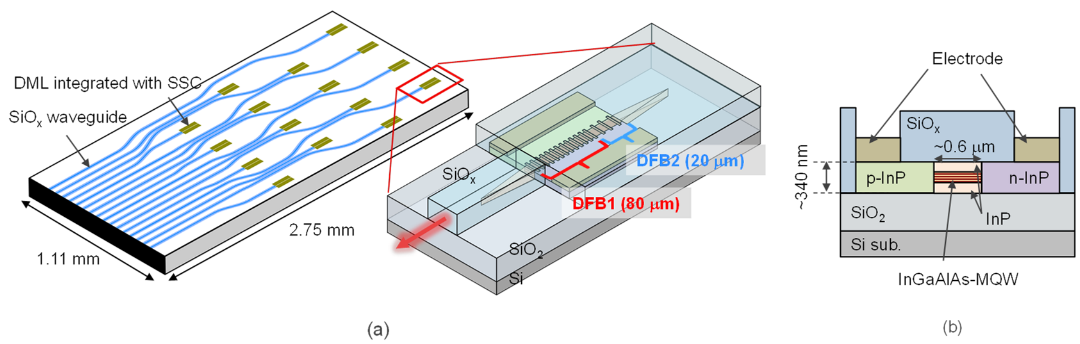

Fig. 1: Schematic drawing of 16-ch membrane DML array on Si integrated with spot-size converter. (b) Cross section of one DML.

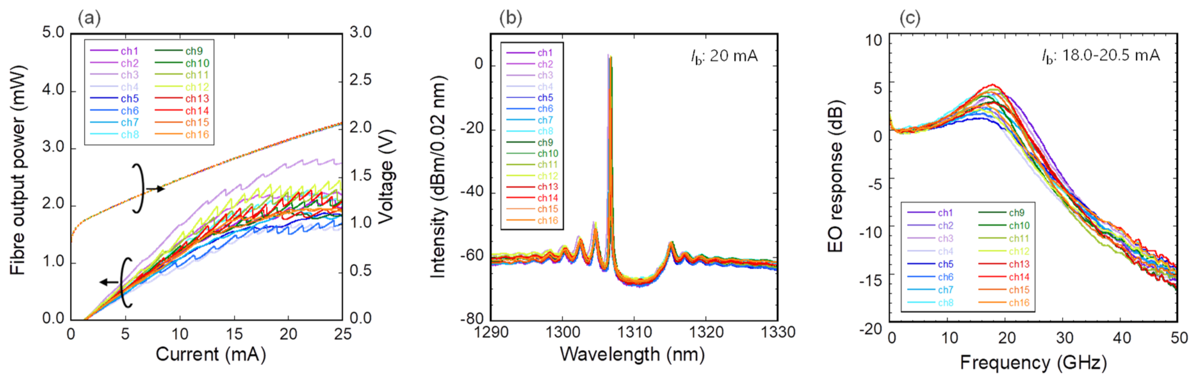

Fig. 2: (a) Light-current-voltage (L-I-V) characteristics of 16-ch membrane DML array. (b) Lasing spectra of 16-ch membrane DML array. (c) Electro-optic (EO) frequency responses.

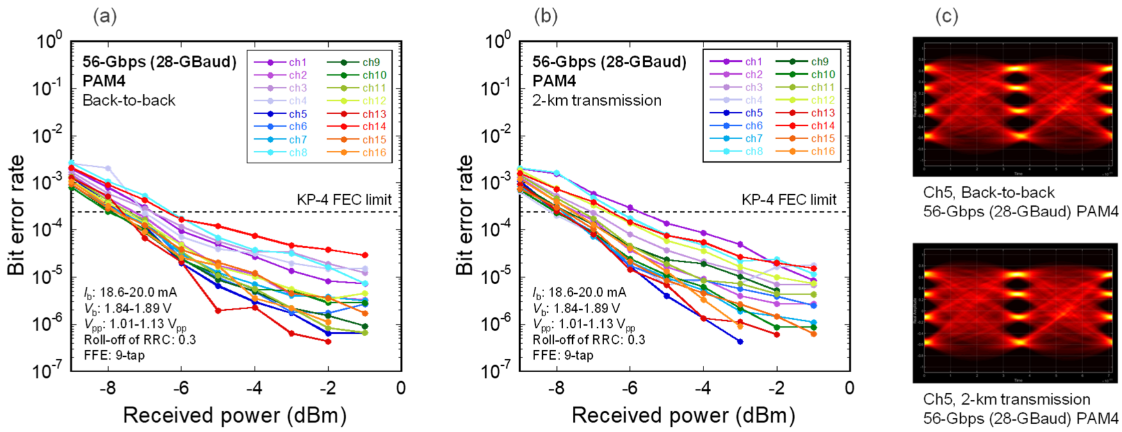

Fig. 3: (a) Back-to-back BER curves for 56-Gbps (28-GBaud) PAM-4. (b) 2-km transmission BER curves for 56-Gbps (28-GBaud) PAM-4. (c) Eye diagrams before and after 2-km transmission.

by ion implantation of Si. The grating was formed on the top of the III-V membrane layer by etching the InP cap. To achieve single-mode lasing with asymmetric optical outputs, we designed a 100-μm-long distributed-feedback (DFB) grating comprising a 80-μm-long front-side section and 20-μm-long back-side section with wavelength detuning [6]. After the formation of the InP mesa on SiO_2, Ti- and Pt-based non-alloy electrodes and Au-based pad electrodes were formed [7]. Finally, a SSC consisting of the InP taper, a SiO_x-waveguide covering the taper, and a SiO_2 cladding layer was integrated.

Laser characteristics

To characterize the fabricated DMLs, we drove them individually and detected the light output from the front facet by butt-coupling the HNAF. The laser chip was put on a stage controlled to 25°C. Figure 2 (a) shows the fibre output power and bias voltage of the 16-ch DMLs with bias current applied. Note that the insertion losses of the isolator and 95/5 ratio coupler are not subtracted. All DMLs exhibited continuous-wave operation with a threshold current smaller than 1.3 mA. The average loss of the fibre coupling and SSC was −1.74 dB. The average differential resistance was 37.3 Ω with a bias current (I_b) of 20 mA. Figure 2 (b) shows the lasing spectra of the DMLs with I_b = 20 mA. All DMLs exhibited single-mode lasing at around 1307 nm, with a wavelength variation of ~0.5 nm. Frequency responses of the DMLs are shown in Fig. 2 (c). The average relaxation oscillation frequency (f_r) and −3 dB bandwidth (f_{3dB}) were estimated to be 19.9 and 25.7 GHz, respectively.

2-km transmission of 28/56-Gbaud PAM-4

We measured the BER of this 16-ch DML array with a 56-Gbps (28-GBaud) PAM-4 signal. Grey-encoded PAM symbols were generated at 84 giga-samples/second by using an arbitrary waveform generator (Keysight AWG M8196A) with an analogue bandwidth of ~32 GHz. A root-raised cosine filter with 0.3 roll-off was applied for pulse shaping. The signal was then amplified electrically through a linear radio frequency (RF) amplifier with 22-dB gain and 60-GHz bandwidth. The modulated signal was added to the direct current via a bias-tee (65-GHz bandwidth) and injected to each DML via an RF probe (67-GHz bandwidth). The output light was launched into the HNAF by butt-coupling it to the SSC. Photodetection was carried out using a commercial 40-GHz *p-i-n* photodiode integrated with a trans-impedance amplifier. The signal was then stored at 160 giga-samples/second using a real-time digital storage oscilloscope with 63-GHz bandwidth for offline processing. For digital signal processing at the receiver, a 9-tap, linear feed-forward equalizer (FFE) was used. Note that no pre-emphasis/pre-equalization was used at the transmitter side.

The BER curves at 56-Gbps (28-GBaud) PAM-4 before and after 2-km transmission are shown in Figs. 3 (a) and (b). The representative eye diagrams before and after 2-km transmission are also shown in Fig. 3 (c). The bias currents for the DMLs were from 18.6 to 20.0 mA with a bias voltage of 1.84–1.89 V and voltage swing of 1.01–1.13 V_{pp}. The corresponding laser-operating energy cost, a product of bias current and bias voltage divided by the bitrate, was 0.66 pJ/bit. The BERs were lower than the KP-4 FEC limit (2.4×10^{-4}) at received optical powers (ROPs) greater than –5 dBm. The power penalty was negligibly small because of the dispersion-free wavelength. The bandwidth density of the 16-ch DML chip reached 807 Gbps/mm.

We also confirmed electrical crosstalk using a multi-channel RF probe. Figure 4 shows the BER curves of ch6 after 2-km transmission with and without driving adjacent channels. The power penalty due to the electrical crosstalk was negligibly small.

Finally, to further increase the data rate, we also demonstrated 2-km transmission using 112-Gbps (56-GBaud) PAM-4 signals. In this experiment, a 31-tap FFE and reduced-complexity 21-tap non-linear equalizer with only 2nd- and 3rd-order polynomial terms and ten 2nd-order Volterra cross-beating terms were used at the receiver side [8]. Figure 5 (a) shows the BER curves of four channels that have different lengths of SiO_x waveguides. Figure 5 (b) compares the BERs of all 16-ch DMLs at the ROPs of 0-0.5 dBm, before and after the 2-km transmission. The eye diagrams after 2-km transmissions are also shown in Fig. 5 (c). We achieved a BER smaller than the KP-4 FEC limit for all channels with 112-Gbps (56-Gbaud) PAM-4. The bandwidth density reached 1.6 Tbps/mm with the laser-operating energy cost of 0.33 pJ/bit.

Conclusions

We developed a 16-ch membrane DML array using non-alloy contact electrodes, integrated with SSCs on Si. We confirmed a low threshold current of less than 1.3 mA, average f_{3dB} of 25.7 GHz with a bias current of only 18.0–20.5 mA, and efficient fibre coupling with an average loss of –1.72 dB. The bandwidth density of the 16-ch DML chip reached 807 Gbps/mm for 56 Gbps and 1.6 Tbps/mm for 112 Gbps PAM-4 signals. Thanks to the membrane III-V structure on SiO_2, we achieved the energy cost of 0.66 pJ/bit for 56 Gbps and 0.33 pJ/bit for 112 Gbps. These results indicate that our fabrication scheme and the membrane devices are attractive for manufacturing PICs for efficient light sources in future datacentre networks.

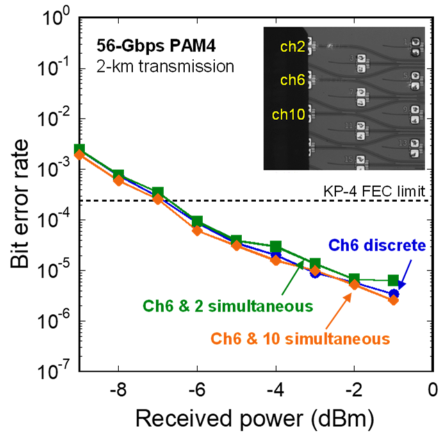

Fig. 4: BER curves of 2-km transmission with and without driving adjacent channels.

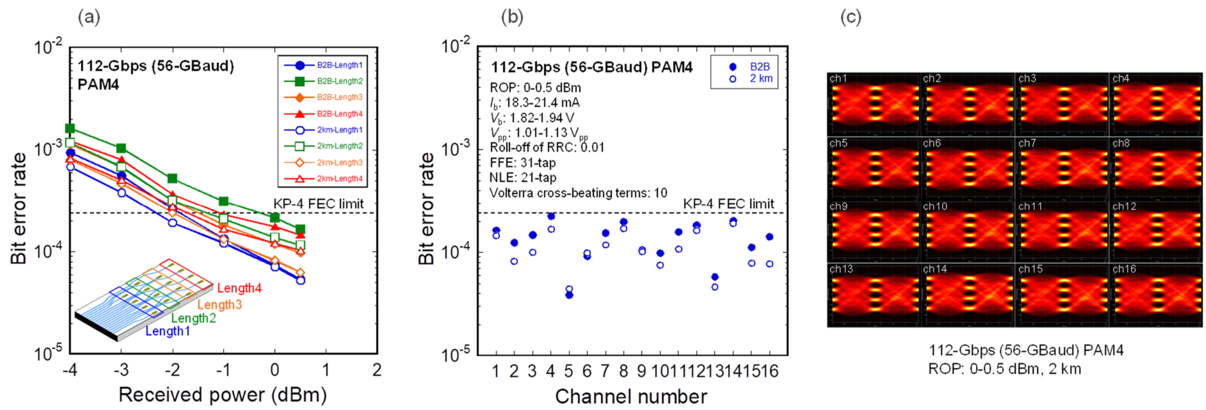

Fig. 5: (a) Back-to-back and 2-km transmission BER curves with 112-Gbps (56-GBaud) PAM-4 for 4 DMLs that have different waveguide lengths. (b) BERs of all 16-ch DMLs at ROP of 0-0.5 dBm. (c) 16-ch, 112-Gbps (56-GBaud) eye diagrams after 2-km transmission.

References

[1] S. Matsuo, T. Fujii, K. Hasebe, K. Takeda, T. Sato, and T. Kakitsuka, “Directly modulated buried heterostructure DFB laser on SiO_2/Si substrate fabricated by regrowth of InP using bonded active layer,” *Opt. Express*, vol. 22, no. 10, p. 12139, 2014, DOI: 10.1364/oe.22.012139.

[2] T. Fujii, K. Takeda, N.-P. Diamantopoulos, E. Kanno, K. Hasebe, H. Nishi, R. Nakao, T. Kakitsuka, and S. Matsuo, “Heterogeneously Integrated Membrane Lasers on Si Substrate for Low Operating Energy Optical Links,” *IEEE J. Sel. Top. Quantum Electron.*, vol. 24, no. 1, p. 1500408, 2018, DOI: 10.1109/JSTQE.2017.2778510.

[3] H. Nishi, K. Takeda, T. Tsuchizawa, T. Fujii, S. Matsuo, K. Yamada, and T. Yamamoto, “Monolithic Integration of InP Wire and SiO_x Waveguides on Si Platform,” IEEE Photonics J., vol. 7, no. 5, p. 4900308, 2015, DOI: 10.1109/JPHOT.2015.2477511.

[4] T. Fujii, K. Takeda, Y. Maeda, T. Sato, T. Tsuchizawa, T. Segawa, and S. Matsuo, “Direct Modulation of 16-ch Two-Dimensionally Arrayed Membrane Lasers on Si,” presented at *2022 28th International Semiconductor Laser Conference (ISLC)*, Matsue, Japan, 2022, DOI: 10.23919/ISLC52947.2022.9943403.

[5] IEEE 802.3 bs, IEEE Standard for Ethernet - Amendment 10: Media Access Control Parameters, Physical Layers, and Management Parameters for 200 Gb/s and 400 Gb/s Operation. 2017, DOI: 10.1109/IEEESTD.2017.8207825

[6] T. Fujii, K. Takeda, H. Nishi, N.-P. Diamantopoulos, T. Sato, T. Kakitsuka, T. Tsuchizawa, and S. Matsuo, “Multiwavelength membrane laser array using selective area growth on directly bonded InP on SiO_2/Si,” *Optica*, vol. 7, no. 7, p. 838, 2020, DOI: 10.1364/optica.391700.

[7] K. Chen, T. Enoki, K. Maezawa, K. Aral, and M. Yamamoto, “High-Performance InP-Based Enhancement-Mode HEMTs Using Non-Alloyed Ohmic Contacts and Pt-Based Buried-Gate Technologies,” *IEEE Trans. Electron Devices*, vol. 43, no. 2, pp. 252–257, 1996, DOI: 10.1109/16.481725.

[8] N.-P. Diamantopoulos, H. Nishi, W. Kobayashi, K. Takeda, T. Kakitsuka, and S. Matsuo, “On the Complexity Reduction of the Second-Order Volterra Nonlinear Equalizer for IM/DD Systems,” *J. Light. Technol.*, vol. 37, no. 4, pp. 1214–1224, 2019, DOI: 10.1109/JLT.2018.2890118.