NbN Waveguide-Integrated Superconducting Nanowire Single-Photon Detectors on 200 mm SOI Wafers

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We demonstrate NbN-based waveguide-integrated superconducting nanowire single photon detectors fabricated on 200 mm SOI wafers using a fully CMOS-compatible process. We achieve 81 % efficiency at 100 Hz dark count rate, 3.2 ns decay time and 200 MHz maximum count rate.

Photon-based quantum information applications such as quantum communications and computing require a scalable, compact and low-cost technology for future widespread deployment [1]. Silicon photonics is a highly attractive technology platform for this purpose, offering the possibility to implement several key functionalities such as photonic qubit generation, coherent manipulation, encoding and detection [2].

Superconducting nanowire single photon detectors (SNSPDs) achieve best-in-class performances in terms of detection efficiency, dark count rate and timing performances [3]. Their on-chip integration is crucial to eliminate coupling losses and benefit from their full detection efficiency, which is of utmost importance, especially for quantum computing.

Several demonstrations of waveguide-integrated SNSPDs have been reported on small sample platforms [4]. Among the various superconducting materials suited for single photon detection, niobium nitride (NbN) gathers several assets such as a relatively high operating temperature (> 2 K), a high degree of stability after several thermal cycles and good timing performances [5]. Waveguide-integrated SNSPDs with near-unity efficiency, low timing jitter (< 25 ps) and fast recovery time (< 10 ns) have been demonstrated using Nb-based thin films on top of Si-based waveguides at temperatures in the range 1-1.4 K [6, 7].

In order to unleash the full potential of SNSPDs, it is necessary to develop their integration in the already mature industrial-grade 200 mm silicon photonics platform using a fully CMOS-compatible process to ensure their compatibility with other key components for single photon generation, coherent manipulation and encoding.

In this paper, we describe the fabrication technology developed on 200 mm SOI wafers using a fully CMOS-compatible process. We characterize the fabrication yield and uniformity over 200 mm wafers through the measurement of the resistance of the nanowires at room temperature. Then, we present the characterization results at cryogenic temperature in terms of on-chip detection efficiency, dark count rate and maximum count rate.

Waveguide-integrated SNSPD fabrication technology

Waveguide-integrated SNSPDs rely on the evanescent coupling of incident light propagating through an input waveguide with a superconducting nanowire placed atop the waveguide. The technology cross-section is shown in Fig. 1(a).

We start the fabrication with the patterning of SOI waveguides of 300 nm height and 400 nm width on 200 mm SOI wafers. After encapsulation and planarization down to the waveguide surface, we deposit a thin, 10-nm AlN layer prior to the deposition of a 5 nm superconducting NbN layer. Both materials are deposited by sputtering at a CMOS-compatible temperature below 450°C. The AlN layer is textured along the vertical axis and in turn induces the vertical texturing of the NbN layer, leading to an enhancement of its critical temperature from 5 to 8.7 K, as we demonstrated in a previous work [8].

NbN nanowires of 100 nm width are then patterned on top of the SOI waveguides with various geometries (straight and U-shape) and lengths. Fig.1(b) shows a microscopy picture of a

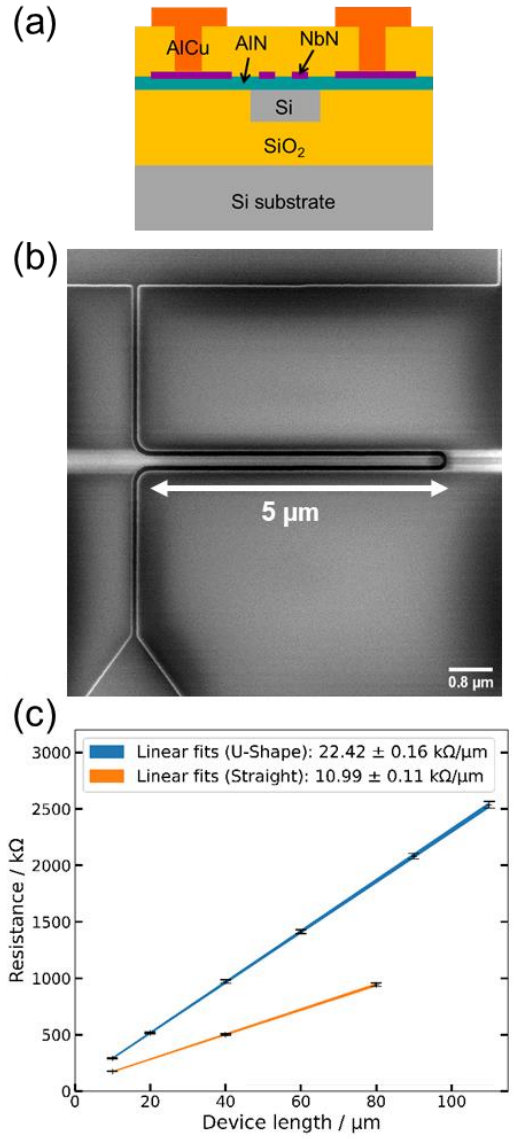

Fig. 1: (a) NbN nanowire technology cross-section. (b) Scanning electron microscopy image of a 5-µm long U-Shape NbN nanowire on top of a Si waveguide using back-scattered electron detector. (c) NbN nanowire resistance as a function of SNSPD device length for straight and U-Shape nanowires, measured on seven dies across the wafer. Black vertical bars indicate statistical measurements over seven chips on the wafer.

U-shape waveguide-integrated SNSPD of 5 µm length. NbN is encapsulated with SiO_2 to prevent oxidation, and the encapsulating layer is planarised. Electrical contacts are obtained with the careful patterning of metallic vias through the encapsulating oxide to preserve the integrity of the thin 5 nm NbN layer and the subsequent deposition and patterning of AlCu contact pads, following a fully CMOS-compatible process.

Characterisation at room temperature

Fig. 1(c) shows the electrical resistance of the fabricated waveguide-integrated SNSPDs as a function of device length for both straight and U-shape nanowires. For each of the nine devices, the measurements were performed on seven dies distributed over the 200-mm diameter wafer. The results show that the resistance is proportional to the device length, with a nanowire linear resistance of 11 kΩ/µm. The standard deviation is below 1 %, showing an excellent fabrication yield and uniformity across the 200 mm wafer, which is a key achievement for such thin nanowires made of polycrystalline material.

Characterisation at cryogenic temperature

After wafer-level testing at room temperature, the wafer is diced into chips for packaging, and for the cryogenic temperature measurements of the detectors figures of merit. The photonic chip is mounted on a copper sample holder using a high thermal conductivity glue.

The chip is then wire-bonded to a PCB test card and pigtailed with a fibre array consisting of standard telecom single mode fibres coupled to the on-chip detectors using integrated grating couplers. The packaged chip is installed in a cryostat brought down to 2.3 K.

In the following, we report the characterisation of a U-shape SNSPD that has a device length of 20 µm (40 µm nanowire length). The first key figure of merit is the On-Chip Detection Efficiency (OCDE), measured using a 1550 nm attenuated laser. It is determined after excluding the grating coupler insertion loss:

$$\mathrm{OCDE} = \frac{\mathrm{PCR} - \mathrm{DCR}}{\gamma_{\mathrm{in}}} \qquad (1)$$

where PCR is the Photon Count Rate, DCR the Dark Count Rate (measured with no incident light) and γ_{in} the incidence photon flux.

A 1550 nm continuous wave laser source is used and its intensity is monitored with a NIST traceable calibrated sensor. A variable attenuator reduces the laser power to create a single photon source equivalent. Finally, the polarization of the incident light is controlled to match the TE polarization of the on-chip grating couplers by maximizing the count rate. The input photon flux (γ_{in}) sent to the detector is estimated to be 100 000 ph/s with a measured relative uncertainty of 2.8 % (2σ).

Fig. 2 presents the on-chip detection efficiency as a function of the biasing current (normalized to the critical current), together with the evolution of dark count rate. The critical current is defined

when an abrupt increase of the OCDE appears, due to the dark counts overwhelming the useful photon flux counts.

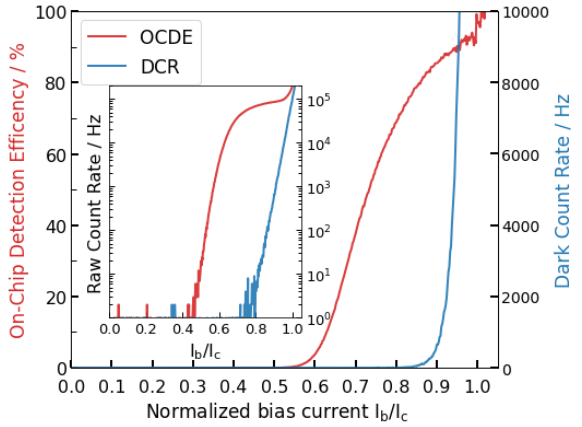

Fig. 2: Left axis: on-chip detection efficiency as a function of biasing current (red). Right axis: detector dark count rate measured vs. biasing current (blue). Inset: raw photon and dark count rate using semi-log Y axis as functions of biasing current. The critical biasing current (I_c) for the SNSPD is 4.62 µA.

The OCDE increases with the biasing current for Ib > 0.5 Ic. No saturation plateau of the photon count rate is observed on Fig. 2. Still, a slope inflexion behaviour of OCDE before the predominance of noise at I_c is noticeable. For a 100-Hz DCR reference, the OCDE is 81.5 ± 2.8 % (at I_b = 0.87 I_c). An 89.7 % detection efficiency can even be obtained, but at the expense of an increased 5-kHz DCR (at I_b = 0.94 I_c) due to the exponential increase of the noise near the critical current. Replacing the first stage room temperature amplifier by a cryogenic version should permit to further reduce the DCR and thus obtain a higher critical current level, leaving a broader biasing range for efficiency increase before the onset of the exponential dark counts increase.

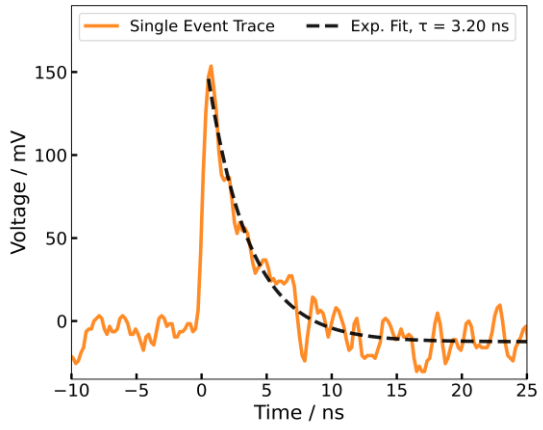

Fig. 3: SNSPD pulse shape for a single detection event (orange). An exponential fit leads to a 3.2 ns decay time (black).

Fig. 3 introduces the pulse shape of a single detection event. This curve decays exponentially, with a short 3.2 ns characteristic time thanks to the short length, hence small kinetic inductance of the detector. Experimentally, our detector was able to measure up to 200 MHz photon flux, with a 50 % OCDE, outputting 100 Mcounts/s, for the same 100-Hz DCR reference.

Conclusions

We present the fully CMOS-compatible fabrication technology of waveguide-integrated SNSPDs on a 200 mm silicon photonics platform, achieving an excellent process uniformity assessed by room temperature resistance non-uniformity as small as 1 % across a wafer.

Thanks to optimized NbN superconducting material deposition using an AlN texturing layer, we achieve a detection efficiency of 81 % when limiting DCR to 100 Hz, a fast decay time of 3.2 ns and a maximum count rate of 200 MHz for a 20-µm long SNSPD device operated at 2.3 K.

Our analysis shows that higher efficiency close to unity should be attainable with better isolation of the photonic chip from dark counts with further improvements of the cryostat.

These results are promising towards the development of a fully integrated quantum photonics platform able to generate, manipulate and detect a large number of photonic qubits for secure communications and quantum computing applications.

Acknowledgements

This work received funding from the French National Agency via the Carnot QPIC project.

Thanks to Dr. Pierre Chausse for helpful discussions and comments.

References

[1] Flamini, Fulvio, Nicolò Spagnolo, and Fabio Sciarrino. “Photonic Quantum Information Processing: A Review”, *Reports on Progress in Physics* 82, nº 1: 016001, 2018, DOI: 10.1088/1361-6633/aad5b2.

[2] Wang, Jianwei, Fabio Sciarrino, Anthony Laing, and Mark G. Thompson. "Integrated Photonic Quantum Technologies”, *Nature Photonics* 14, nº 5: 273-84, DOI: 10.1038/s41566-019-0532-1.

[3] Reddy, Dileep V., Robert R. Nerem, Sae Woo Nam, Richard P. Mirin, and Varun B. Verma. “Superconducting Nanowire Single-Photon Detectors with 98% System Detection Efficiency at 1550 nm”, *Optica* 7, nº 12: 1649-53, 2020, DOI: 10.1364/OPTICA.400751.

[4] Ferrari, Simone, Carsten Schuck, and Wolfram Pernice. “Waveguide-Integrated Superconducting Nanowire Single-Photon Detectors”, *Nanophotonics* 7, nº 11: 1725-58, DOI: 10.1515/nanoph-2018-0059.

[5] Gol'tsman, G. N., O. Okunev, G. Chulkova, A. Lipatov, A. Semenov, K. Smirnov, B. Voronov, A. Dzardanov, C. Williams, and Roman Sobolewski. "Picosecond superconducting single-photon optical detector", *Applied Physics Letters* 79, nº 6: 705-7, DOI: 10.1063/1.1388868.

[6] Pernice, W. H. P., C. Schuck, O. Minaeva, M. Li, G. N. Goltsman, A. V. Sergienko, and H. X. Tang. "High-Speed and High-Efficiency Travelling Wave Single-Photon Detectors Embedded in Nanophotonic Circuits", *Nature Communications* 3, nº 1: 1325, DOI: 10.1038/ncomms2307.

[7] Wolff, Martin A., Fabian Beutel, Jonas Schütte, Helge Gehring, Matthias Häußler, Wolfram Pernice, and Carsten Schuck. "Broadband waveguide-integrated superconducting single-photon detectors with high system detection efficiency", *Applied Physics Letters* 118, nº 15: 154004, DOI: 10.1063/5.0046057.

[8] Rhazi, Raouia, Houssaine Machhadani, Catherine Bougerol, Stéphane Lequien, Eric Robin, Guillaume Rodriguez, Richard Souil, and al. "Improvement of Critical Temperature of Niobium Nitride Deposited on 8-Inch Silicon Wafers Thanks to an AlN Buffer Layer", *Superconductor Science and Technology* 34, nº 4: 045002, DOI: 10.1088/1361-6668/abe35e.