

Wafer Scale Fabrication of Multi-Plane Light Conversion Devices

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Abstract We fabricate and measure compact 45 mode spatial mode multiplexers based on multi-plane light conversion technology compatible with wafer scale manufacturing and measurement. The devices measure $2 \times 4.8 \times 1$ mm in dimension, fibers can be directly attached and work over 200 nm bandwidth around 1550 nm. ©2023 The Author(s)

Introduction

The continuing growth in demand for optical transport capacity drives the need to expand optical systems to use more than the single spatial mode of conventional fiber. Mass-producible, inexpensive, compact, and easily packagable mode multiplexers will be necessary to widely deploy space-division multiplexing in multimode fiber^[1]. None of the existing technologies such as photonic lanterns, 3D waveguides, directional couplers, planar waveguides such as Si photonics, and multi-plane light conversion^{[2],[3]} can easily support 45 modes required for GI-MMF transmission and are easy to package^[4]. Photonic lanterns are built one at a time, 3D waveguides do not produce good multiplexers beyond 3 or 6 modes, and planar waveguides tend to have difficulty exciting 2D mode patterns. Multi-plane light conversion devices can support a large number of modes^[5], but tend to be large free space devices that are challenging to package with fibers. The MPLC systems comprise phase masks separated by free-space propagation, which requires precise alignment and high mechanical and thermal stability.

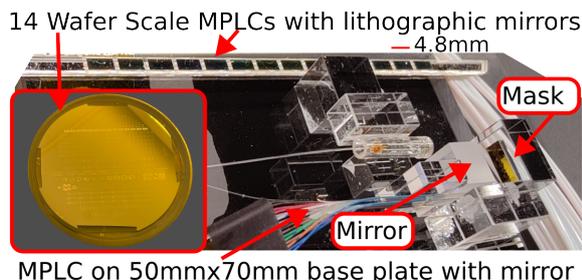


Fig. 1: Comparison of internal MPLC devices and a free-space MPLC device. The single MPLC packaged in free-space requires a very difficult alignment between the mirror and the MPLC to form a perfectly flat cavity. Internal device is compatible with wafer scale testing and only requires fiber attach.

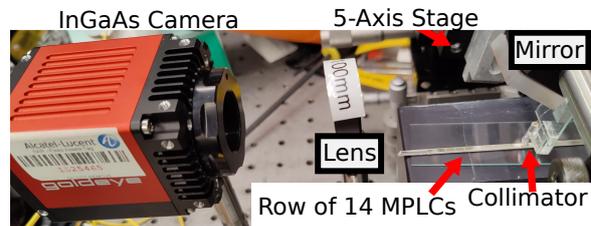


Fig. 2: Experimental setup for characterization. The MPLC is laid flat and a 5-axis stage is used to scan a collimator to each input. The output is directed towards a camera using a mirror and lens.

Wafer Scale Platform

Here we show how to fabricate an entire wafer of MPLC devices where the free propagation region is inside of the wafer. Using a wafer scale approach converts the individual alignments into a fabrication step within the wafer foundry process. Mirrors are lithographically defined, and the light enters and exits the device on same side so it is compatible with wafer scale testing much like grating couplers in integrated silicon photonic platforms. In addition to the manufacturing advantages of wafer scale fabrication, it also opens up the opportunity to combine these devices with other wafer scale process such as optical filters, silicon photonic devices or electronics. While the primary focus in this work is on devices for coupling to multi mode fibers for communications applications, the creation of an integration platform for MPLC's potentially opens up many other use cases, in free space communication systems, sensing, beam shaping, imaging, microscopy and astronomy^[6]. The closest other device demonstrated supports 3 modes and uses polarization sensitive metasurfaces^[7] which tend to have higher losses than gray-scale but have fewer lithographic steps.

The phase masks are fabricated using a multi-step gray scale lithography on 100mm fused silica wafers that are 1mm thick. The wafer thick-

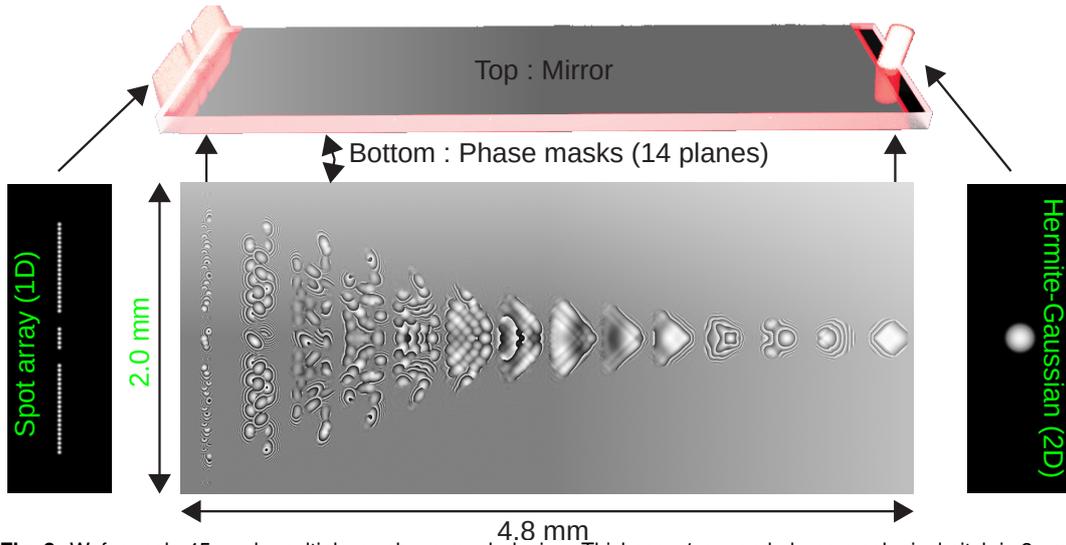


Fig. 3: Wafer scale 45 mode multiplexer phase mask design. Thickness 1mm and phase mask pixel pitch is 2 μ m.

ness was chosen to be compatible with the physical fabrication requirements while also matching to beam path lengths that were consistent with the phase masks resolutions available from the fabrication process. The process consists of 6 binary phase etches of doubling phase step produce to 64 phase levels between 0 and 3π and the lithography supported a 2 μ m pixel pitch. The backside is patterned with photo-resist to define the plane mirrors and the entrance and exit apertures. The high reflectivity is achieved on both the phase mask and plane mirror by evaporating silver mirrors on both sides of the wafer. Liftoff removed the unwanted metal to define the input and output apertures. While in principle the fabricated devices could be tested at wafer-scale we diced out and tested one row of 14 mode multiplexers.

Design

As an initial test of this platform we fabricate a variety of MPLC designs. We characterise the 45-mode multiplexer device which converts 45 beams in a linear array to 45 Hermite-Gaussian (HG) modes (i.e., GI MMF modes in the Cartesian coordinate system). This design is similar to the 45-mode multiplexer we have described previously^[8] which allows us to evaluate the advantages and limitations of the wafer scale approach. It differs in that it is designed for propagation inside the 1 mm thick fused silica wafer and uses 48 phase steps out of the available 64. Figure 3 shows the 14 phase masks to transform the modes. Additionally, the inputs and outputs are the fibers as opposed to having collimation micro lenses attached to the fibers. The function of these micro lenses are effectively incorporated into the first phase masks. This removes the com-

plexity of assembly of aligning micro lens arrays to fiber arrays. The input side accepts 45 single mode spots with waists of 6.6 μ m located at the mask. Internally, the beam angle is 10 degrees which forms an external angle to free-space of 14 degrees. The output modes are Hermite-Gaussian with a ω_0 of 30.0 μ m.

Most of the device fans the array of spots into a triangular arrangement which then very efficiently produces the Hermite-Gaussian modes. Starting from the triangular input could reduce the required phase planes as shown in^[3]. Optimization of the design uses primarily wavefront matching which is a subset of inverse design^[9] that optimizes the power coupling between each input and output mode. Most of the phase masks are smooth which eases fabrication of gray scale features and increases the operation bandwidth. Phase wraps and high spatial frequency structure tend to introduce scattering.

Figure 5a) shows a simulation of this design assuming that the wafer thickness is not precise and Fig. 4a) shows the simulated modes along with the measured modes at 1550nm. Simulation results are computed by first building the complex transfer matrix [Fig. 5b)] by computing overlap integrals of the simulated output modes to the target modes. The total power of the matrix is the insertion loss, and the mode dependent loss is calculated by a singular value decomposition which finds the maximum possible transmission through the system and the minimum. The crosstalk, defined as the power in diagonal compared to power outside the diagonal, is between 9-11dB across 200 nm.

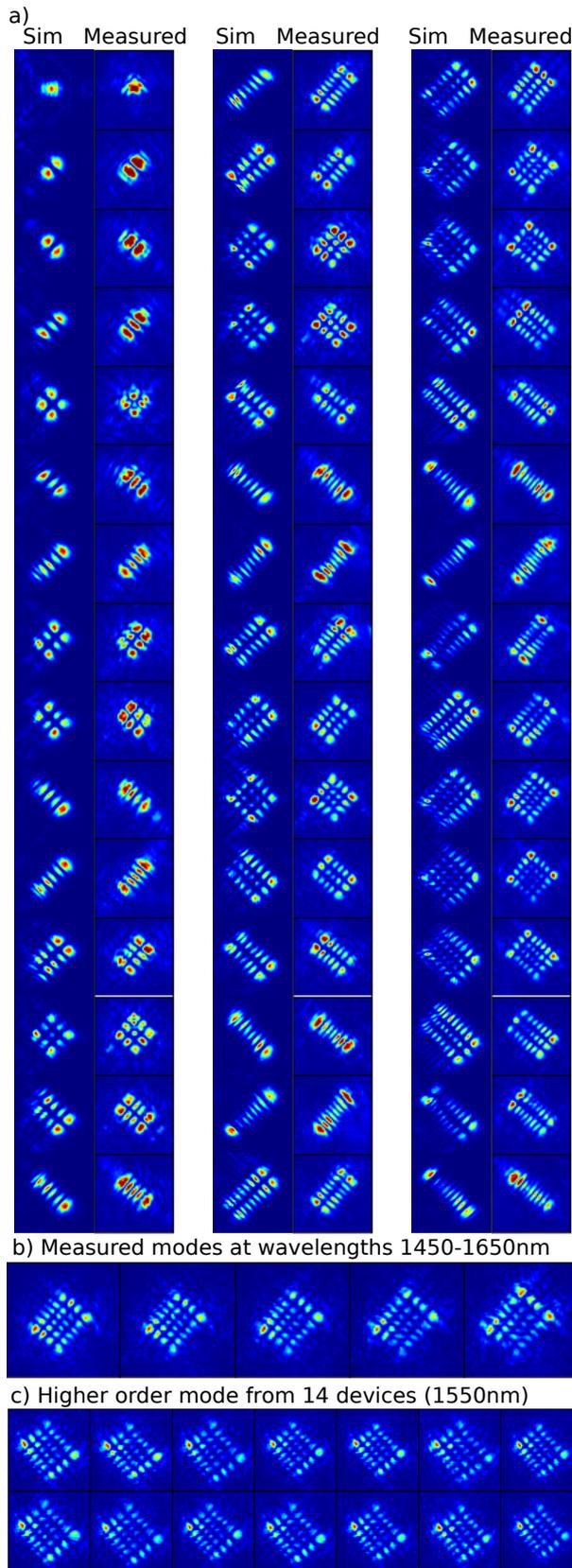


Fig. 4: a) Measured mode profiles at 1550 nm compared to simulation. b) Wavelength scan. c) Waferscale testing.

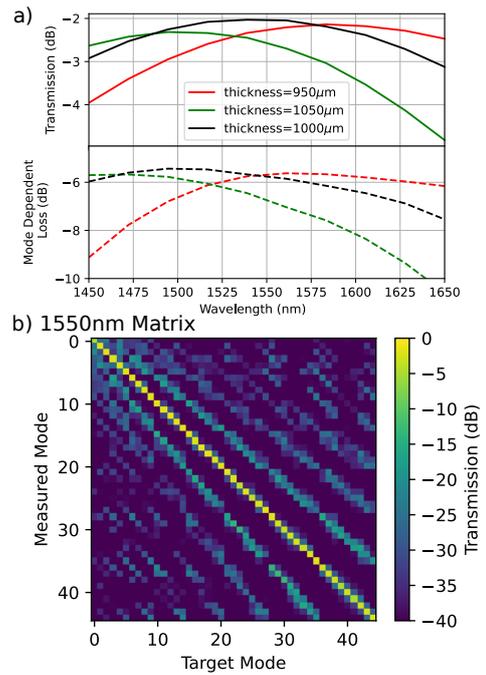


Fig. 5: Simulation of 45mode MPLC designed for a 1000 μ m thick substrate. a) Transmission and mode dependent loss vs thickness. b) Transmission matrix for 1000 μ m at 1550 nm.

Results and Comparison to Design

Figure 4 shows the mode intensity measured by translating a collimator across the inputs. The collimator is an AR coated SMF pigtail glued inside a ferrule with a 0.29mm pitch grin lens. The grin lens is positioned to project a 6.6 μ m waist 2 mm from the grin lens facet which enables us to couple through 1mm of glass to the phase mask without need to make contact with the wafer.

Figure 4a) shows the measured mode profiles in comparison to the simulations, and demonstrates good mode fidelity. Figure 4b) demonstrates broadband operation and Figure 4c) demonstrates consistency across the wafer. The insertion loss is 7dB (2-dB theoretical, 27 bounces off of Ag coated, and a lot of scatter from fabrication tolerances). These results show the device performance is essentially equivalent to the previous non-integrated device^[8]. Insertion loss are expected to reduce to 2-3 dB from fabrication improvements such as smoother gray scale lithography and better coatings.

In conclusion, we have demonstrated a wafer scale approach to the fabrication of MPLC which bring several benefits. It simplifies the assembly and packaging. It allows wafer scale testing. It opens the opportunity for wafer scale integration with other wafer scale technologies. We have demonstrated that there is no performance degradation with this approach, by constructing and testing a 45 mode multiplexer.

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