

Low-Complexity Architecture for Soft-Output Trellis-Based Detection in High-Speed Data Center Applications

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Abstract *An architecture enabled by DFE is proposed to achieve reduced-state trellis-based algorithms for data center applications. Performance evaluation using PAM-4 IM/DD experimental data shows that the penalty due to state pruning is below 0.5 dB, while a complexity reduction up to 57% is achieved.*

Introduction

Non-binary pulse amplitude modulation (PAM) and soft decision (SD)-forward error correction (FEC) are promising techniques for boosting the speed of intensity-modulation (IM)/direct-detection (DD) links^{[1],[2]} in applications such as intra- and inter-data center interconnects. Recently, an SD concatenated code has been adopted as the optical interconnect FEC in 200 Gb/s PAM-4 serial intra-data center applications^[3]. To take full advantage of SD-FEC, accurate computation of bit-wise log-likelihood ratios (LLRs) is crucial. However, inter-symbol interference (ISI) caused by bandwidth-limited components limits the LLR accuracy under the additive white Gaussian noise (AWGN) assumption^[4].

Traditional approaches to mitigate ISI are filters, and trellis-based algorithms targeting symbol-wise maximum a posteriori (MAP) detection. Within the former category, we find decision-feedback equalization (DFE). DFE is easy to implement, but it suffers from error propagation. The resulting burst errors can significantly penalize the performance of SD-FEC. Therefore, it is important to mitigate this burst error penalty^[5]. Bit interleaving or precoding based on differential and modulo operations^{[5],[6]} are commonly used to reduce the penalty. However, interleaving might cause high latency, and precoding prevents accurate LLR due to the modulo errors^[7]. The trellis-based solutions include Log-MAP (LM), Max-Log-MAP (MLM)^[8] and soft-output Viterbi algorithm (SOVA)^{[9]–[11]}. These algorithms provide (near-)optimum performance, but with very high complexity. Various state pruning methods have been proposed for VA^{[12]–[15]}, however, these do not provide soft-outputs for SD-FEC.

In this paper, we propose to combine DFE

with trellis-based algorithms, based on a trellis characterizing DFE burst errors^[16]. In this proposed architecture, instead of the M -ary PAM symbols, only 3 typical DFE symbol errors need to be tracked. The error information is then used to generate LLRs in a modified demapper. The proposed architecture reaches a tradeoff: (i) the complexity of trellis-based algorithms is reduced and (ii) the burst error penalty is mitigated. Compared to our previous work^[16], here we manage to apply the trellis in^[16] to practical soft-output algorithms (i.e., MLM and SOVA) and investigate their performances in experiments.

From the PR Channel to DFE-3 States

We consider a one-tap partial response (PR) channel for modeling the ISI in IM/DD links^[17]. At time i , given the transmitted symbol x_i , the received symbol is $y_i = x_i + hx_{i-1} + n_i$, where h is the tap coefficient and n_i is AWGN. The set of PAM- M symbols is defined as $\mathcal{X} \triangleq \{\pm 1\Delta, \pm 3\Delta, \dots, \pm(M-1)\Delta\}$.

Given received symbols $\mathbf{y} = [y_1, y_2, \dots, y_N]$, the symbol-wise MAP rule computes the a posteriori probability (APP) $P(x_i = x|\mathbf{y})$, which is later converted into LLRs for decoding. Traditional trellis-based algorithms characterize all possible ISI states (M for the one-tap PR channel) and their transitions. By unfolding the M states in time, a fully-connected trellis is obtained, where each path represents a possible transmitted symbol sequence $\mathbf{x} = [x_1, x_2, \dots, x_N]$. An illustration of the PAM-4 trellis is shown in Fig. 1 (a).

DFE removes ISI from the current received symbol by using previous hard decisions (HDs). Given the HD \hat{x}_{i-1} , the equalized symbol is $\bar{y}_i = y_i - h\hat{x}_{i-1}$, which determines the next HD \hat{x}_i . With the equalized symbols $\bar{\mathbf{y}} = [\bar{y}_1, \bar{y}_2, \dots, \bar{y}_N]$, an AWGN demapper computes their LLRs as if all ISI has been removed. However, this assumption

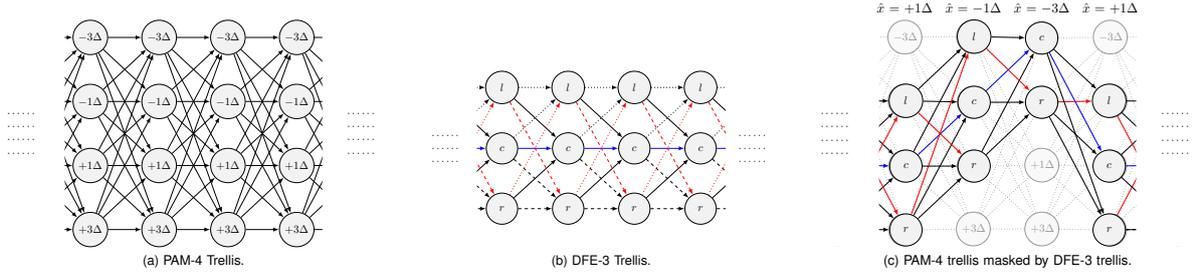


Fig. 1: (a) the PAM-4 trellis; (b) the DFE-3 trellis; (c) shows an example of (b) given certain HD input on top of (a).

is not always true, since error propagation can occur if an HD is incorrect. We define the error as $e_{i-1} \triangleq x_{i-1} - \hat{x}_{i-1}$, where $e_{i-1} \neq 0$ leads to a biased observation \bar{y}_i , causing \hat{x}_i to be more prone to errors, i.e., $\bar{y}_i = x_i + n_i + h e_{i-1}$.

For PAM- M , there are $(2M-1)$ possible errors. At relatively high signal-to-noise ratios (SNRs) and small h , most errors occur between adjacent symbols. Therefore, we consider a reduced number of errors $e_{i-1} \in \{0, \pm d\}$, where $d = 2\Delta$. These 3 errors lead to different *biased states* s_i for \bar{y}_i , which are written as

$$s_i \triangleq \begin{cases} l, & \text{if } e_{i-1} = -d \\ c, & \text{if } e_{i-1} = 0 \\ r, & \text{if } e_{i-1} = +d \end{cases},$$

where $s_i \in \mathcal{S} \triangleq \{l, c, r\}$, and we call them “DFE-3 states”. The corresponding trellis is depicted in Fig. 1 (b). DFE error propagation is indicated by the red edges between l and r . The red edges being dotted/dashed implies that the transitions to l and r might have zero state transition probability and thus cause disconnections.

The proposed DFE-3 trellis in Fig. 1 (b) can be deemed as a PAM- M trellis after pruning states, thanks to the pre-processing of DFE. Fig. 1 (c) shows an example of the DFE-3 trellis on top of the PAM-4 trellis, given a certain input of HD \hat{x} . The center state c falls upon the HD, and the disconnection to l takes place when c happens to be the leftmost symbol -3Δ . In general, the DFE-3 trellis leads to a simpler analysis than the PAM- M trellis, because (i) the number of states decreases from M to 3 and (ii) part of transitions are disconnected, and thus, they can be ignored.

Detection and Demapping with DFE-3 States

In the proposed architecture, the DFE-3 trellis is used to obtain the state APP $P(s_i = s' | \bar{\mathbf{y}})$. The key to this APP is computing the state transition probability, as has been explained in^[16]. Here we compute this probability in the log domain to ensure compatibility with LM, MLM and SOVA.

Once $P(s_i = s' | \bar{\mathbf{y}})$ are calculated, they are used in a state-based demapper to account for the bias

imposed on \bar{y}_i . The DFE-3 state LLR is defined as

$$L_{i,j}^S \triangleq \log \frac{\sum_{s' \in \mathcal{S}} \sum_{x \in \mathcal{X}_j^1} p(\bar{y}_i | s_i = s', x_i = x) P(s_i = s' | \bar{\mathbf{y}})}{\sum_{s' \in \mathcal{S}} \sum_{x \in \mathcal{X}_j^0} p(\bar{y}_i | s_i = s', x_i = x) P(s_i = s' | \bar{\mathbf{y}})},$$

where $\mathcal{X}_j^b \subset \mathcal{X}$ are the set of symbols labeled by bit $b \in \{0, 1\}$ at bit position j . The LLRs are calculated by using Jacobian logarithm for LM, or Max-Log approximation for MLM and SOVA. Note that in^[16], state LLR is computed instead with $P(s_i = s' | \bar{\mathbf{y}}')$, where $\bar{\mathbf{y}}' = [\bar{y}_1, \bar{y}_2, \dots, \bar{y}_{i-1}]$.

Experimental Results and Discussions

For baseline comparisons, the following schemes are considered: (i) DFE; (ii) DFE with random bit-interleaving within each codeword; (iii) DFE and precoding; (iv) PAM-4 trellis-based algorithms (LM, MLM, and SOVA). Regarding scheme (iii), after de-precoding the HDs, the demapper uses a numerically optimized lookup table to map the output into LLR^[18]. The proposed DFE-3 trellis-based algorithm requires DFE and the state-based demapper. The traceback length of SOVA is set as 10 regardless of the trellis in use. The LDPC code from IEEE 802.3ca with blocklength 17664 bits and rate 0.83 is employed. The decoder performs belief propagation (BP) with 6 iterations.

The performances of the aforementioned schemes are evaluated offline by using the recorded data from PAM-4 IM/DD experiments. The offline processing and experimental setup are depicted in Fig. 2. In the offline generation, 2^{15} bits from a pseudo-random bit sequence (PRBS) are mapped to symbols for transmission.

The experiments target 100G serial links with a rate of 53.125 GBaud. The memory size of the DSP chip is 16 Kbytes. In addition, the testbed suffers from high insertion loss caused by lossy/long electrical traces (e.g., between DAC and driver) and bandwidth limitation. After transmission, noise whitening and feedforward equalization (FFE) are performed. By treating the effective channel as PR channel, h is estimated to be 0.66. The discrepancy between the PR and the real channel is due to the residual ISI after FFE.

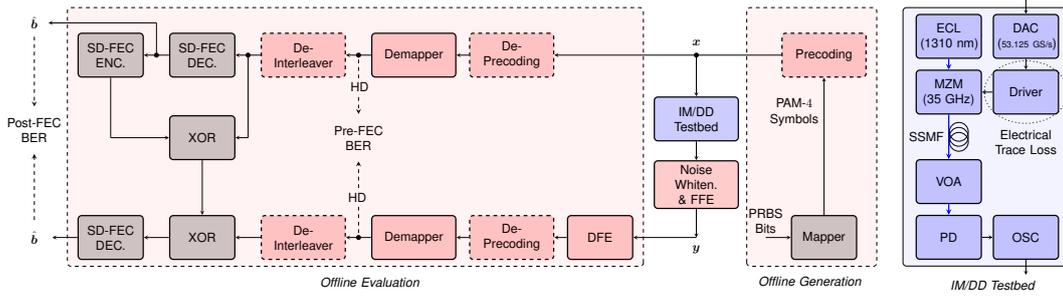


Fig. 2: Block diagrams of PAM-4 IM/DD experiment and offline processing. The dashed pink blocks indicate optional DSPs, depending on the considered schemes. ECL: external cavity laser; DAC: digital-to-analog converter; MZM: Mach-Zehnder modulator; SSMF: standard single-mode fiber; VOA: variable optical attenuator; PD: photo diode; OSC: oscilloscope.

The offline evaluation of the pre/post-FEC BER is based on an emulation approach^{[19],[20]}. In the upper left corner of Fig. 2, scrambling (achieved by XOR operations) and re-encoding are conducted to convert the PRBS-generated codeword into a real codeword. To sweep different SNR values, noise loading is used. SNR is defined as $(1 + h^2)/\sigma^2$ with unitary signal power.

Fig. 3 (a) shows the pre-FEC BER vs. SNR performance. Precoding offers the best performance in correcting burst errors, followed by trellis-based algorithms. Using the PAM-4 trellis corrects more errors than the DFE-3 trellis. Surprisingly, LM exhibits worse performance than MLM and SOVA for both trellises. We conjecture that LM is more sensitive than MLM and SOVA to the presence of residual ISI, because LM follows more strictly the AWGN assumption on the additive noise. The fact that LM is more complex, but ends up with worse performance, makes LM less attractive in real IM/DD systems than MLM and SOVA. DFE, with or without interleaving, shows the worst pre-FEC BER. Since interleaving only breaks the correlation between errors, both red curves overlap.

Fig. 3 (b) shows end-to-end results. It can be seen that interleaving slightly improves the performance of DFE. Although precoding provides good pre-FEC BER, as shown in Fig. 3 (a), its post-FEC BER is limited due to the use of discrete LLRs. DFE alone or with interleaving/precoding can never reach a BER of 10^{-6} . On the other hand, Fig. 3 (b) shows the excellent performances of trellis-based solutions, where the smallest gap between the DFE-3 and the PAM-4 clusters is 0.39 dB. In particular, the DFE-3 trellis causes loss within 0.5 dB for SOVA.

Here we present a rough complexity analysis of the processing on the trellis. The number of states, and the number of branches per state, are both M for the PAM- M trellis. By contrast, these numbers are both 3 for the DFE-3 trellis. Hence, the ratio of the PAM- M and the DFE-3 trellis com-

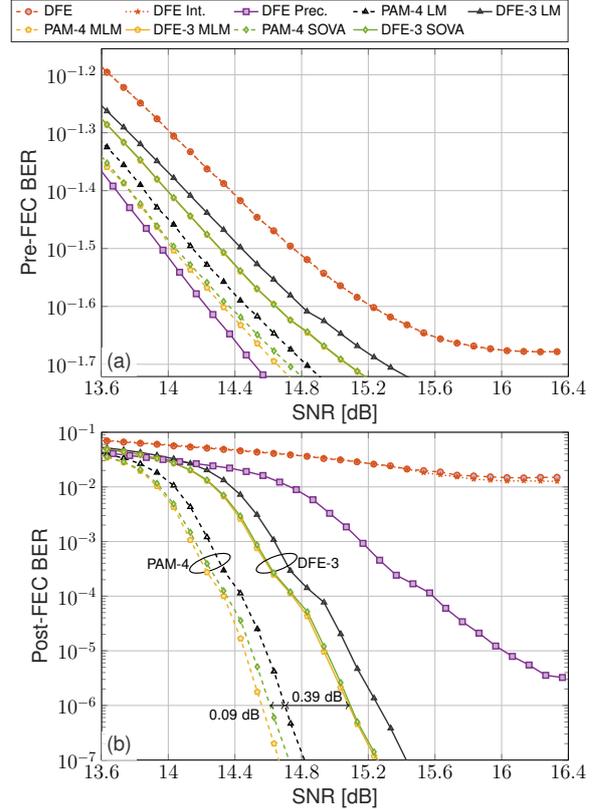


Fig. 3: PAM-4 experimental results: (a) Pre-FEC BER vs. SNR, and (b) Post-FEC BER vs. SNR.

plexity is roughly proportional to $M^2/9$. Specifically, we count the number of add, compare, and select (ACS) operations, which are extensively used in MLM and SOVA. Compared to the PAM-4 trellis, using the DFE-3 trellis reduces the number of ACS by 44% and 57% in MLM and SOVA, resp.

Conclusions

In this paper, we experimentally investigate the performances of several soft-output trellis-based algorithms. The proposed architecture, enabled by the DFE-3 trellis, leverages a performance penalty of less than 0.5 dB to achieve considerable complexity reduction up to 57%. It is believed to be of interest to future data center applications. For instance, with the deployment PAM-8, the complexity reduction can reach 95% for SOVA.

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