

Fast and High-Port-Count Optical Switch using Electro-Optic Silicon-Photonic Switch and Filter Circuit

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Abstract We fabricate a polarization-independent electro-optic Silicon-Photonic circuit that monolithically integrates Mach-Zehnder interferometer switches and filters for creating a fast and high-port-count optical switch. Design integrity of the switch is verified by $3,712 \times 3,712$ switch experiments using 128-Gb/s DP-QPSK signals; switching times are under 55 nanoseconds. ©2023 The Authors

Introduction

Optical switches are deemed to be an attractive way of creating large bandwidth networks for data centres (DCs) and AI/ML applications. In fact, Google recently deployed optical circuit switches in their DCs and reported that they have significantly reduced network power consumption and cost [1]. Present hyperscale DCs rely on multi-stage electrical switching networks. Google used three-dimensional microelectromechanical system (3D-MEMS) optical circuit switches to replace the uppermost electrical switching tier (Spine switches), where data flows are well aggregated and the millisecond switching speeds were acceptable in combination with sophisticated traffic and topology engineering [1]. In order to deepen the use of optical circuit switches and thus maximize the optical benefits, faster switching speed is essential to minimize traffic and topology engineering overheads [2]. Silicon-Photonic switches are a promising candidate to attain this [3–7]. We have already developed switches and tunable filters (TFs) using Symmetric and Asymmetric thermos-optic Mach-Zehnder interferometers (MZIs), respectively, to create several thousand port optical switches, where the available switching speed is just a few microseconds [8]. Using electro-optic MZIs (EO-MZIs) reduces the control latency while maximizing the optical switching network utilization [2].

In this paper, we first analytically investigate switching speeds of Symmetric and Asymmetric MZIs (AMZIs) so that performance of combined switches and filters can be optimized. Our numerical simulations clarify the optimum number of AMZI stages in a TF, considering loss factors and receiver's power limitation. To verify the analyses, we fabricate an on-chip polarization-diversity 32×1 selector and TF. Its performance including insertion loss (IL), polarization dependent loss (PDL), and switching speed are reported. Finally, we demonstrate the integrity of the fabricated device through 128-Gb/s DP-QPSK transmission

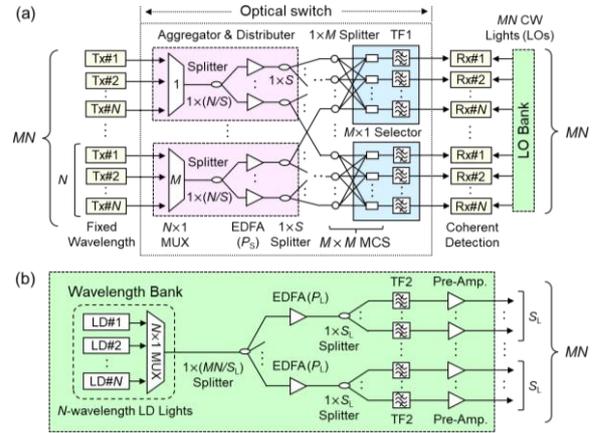


Fig. 1: Configuration of (a) proposed $MN \times MN$ optical circuit switch, including (b) LO bank for coherent detection.

experiments in a $3,712 \times 3,712$ optical switch, where the coherent signals are switched within the response time of 55 ns.

Proposed Optical Switch Architecture

Fig. 1 depicts our proposed $MN \times MN$ optical switch architecture equipped with a shared LO bank for coherent detection. The incident signals from N fixed-wavelength transmitters are aggregated by a $N \times 1$ multiplexer (MUX) and then distributed by a $1 \times (N/S)$ splitter. After loss compensation by EDFAs, the signals are further distributed by $1 \times S$ splitters. An $M \times M$ multicast switch (MCS) splits the input signals at a $1 \times M$ splitter and selects one of the M distributed signal groups with an $M \times 1$ selector. The signals including the target channel are extracted by a tunable filter (TF1). Finally, the target signal in the filtered signal is coherently detected by using a local oscillator (LO) sourced from an LO bank. The LO bank [Fig. 1(b)] uses an optical comb source or aggregated N fixed-wavelength LD lights. Similarity to the signal side, broadcasting LOs are implemented by $1 \times (MN/S_L)$ and $1 \times S_L$ splitters to distribute the WDM channels. An EDFA is placed between the splitters to achieve the output power of P_L dBm. An LO channel is

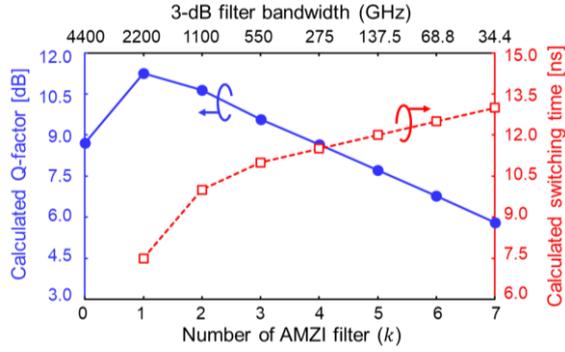


Fig. 2: Q-factor and switching time with $P_s = 24$ dBm and $S = 4$ for different AMZI stages.

extracted by TF2 and amplified with a compact and low-cost preamplifier. Although the EDFA is a relatively expensive device, the per-port cost is reasonable as it is shared among multiple output ports (S or S_L). In this way, the proposed architecture cost-effectively realizes a high-port-count optical switch for coherent signals using LO wavelength selection.

Analyses of Switch Performance and Speed

The MCS port count (M) and switching speed are important parameters that determine optical switch effectiveness. EO-MZI is the key to achieving sub-microsecond switching speeds in Silicon-Photonic devices. To meet the OIF requirement (18-dB receiver dynamic range [9]), even a coherent system needs TF1 to reject the out-of-band (OOB) signals when a large number ($N > 60$) of wavelengths are multiplexed in the C-band (40 nm) [10]. Narrower filters can be formed by concatenating AMZIs; 3-dB bandwidth is given by $4400/2^k$ GHz for a k -stage cascaded AMZI [11]. The multistage AMZI filter mitigates receiver impairment by minimizing OOB noises, but incurs extra loss inside the MCS (e.g., 1 dB loss per EO-AMZI [12]). The switching time also slows with more cascaded AMZI stages, as is evident from TF transmission $P(k) = \prod_{i=1}^k \cos^2(\Delta\varphi)$ with phase shift $\Delta\varphi$ [11]. Due to the larger phase shift required, MCS agility is determined by the AMZI filters not symmetric MZI selectors.

We numerically investigated the signal quality and switching speed dependency on the AMZI filter stages, while maintaining constant port count ($MN = 3,712$) for 128-Gb/s DP-QPSK signals in the C-band. The phase shift $\Delta\varphi$ associated with carrier density changes can be modeled by the travelling-wave [13] and rate (without gain) equations [14]. Except for a carrier lifetime of 5 ns and device sizes detailed in Fig. 3(b), the simulation parameters are the same as those listed in previous works [11, 13, 14]. Fig. 2 plots the calculated Q-factor and switching time (10%–90% rise time) for different numbers of AMZI filter stages of TF1. In the absence of AMZI filters, a 2.5-dB Q-penalty

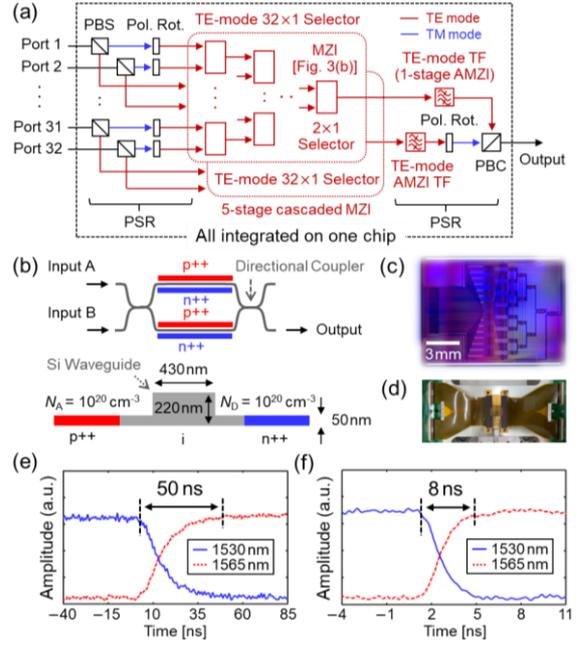


Fig. 3: (a) Schematic of integrated polarization-insensitive 32×1 selector and TF based on (b) EO-MZIs. Photographs of the switch (c) chip and (d) module. Measured transmittance with (e) DACs and (f) pulse generator.

from the optimum value is observed where MCS port count (M) is doubled to compensate for the reduced N ($N \leq 60$) due to the receiver's power limitation. With the AMZI filter, the Q-factor linearly falls as more AMZI stages are used. This is because additional filter losses (i.e., 1 dB/EO-AMZI) dominate the impairment rather than OOB noise. By reducing the stage number from 7 to 1, the switching time can be shortened from 13 ns to 7.5 ns. We therefore chose the AMZI filter stage of $k = 1$ for the MCS.

Fabrication of 32×1 SiPh EO Space Switch

We fabricated a polarization-independent and high-speed Silicon-Photonic space switch based on EO-MZIs. Fig. 3(a) illustrates a schematic configuration of the switch; 33 polarization splitter-rotators (PSRs), 62 MZI element switches and 2 AMZI filters were fabricated on one silicon chip. As in previous works [8, 15], two sets of a TE-mode 32×1 selector and TF are integrated in an on-chip polarization diversity circuit with PSRs. Each selector is formed by 5-stage MZI element switches in tree topology, together with a 1-stage AMZI filter that prevents receiver power saturation. As shown in Fig. 3(b), the element switches have a pair of 3-dB directional couplers and two arms of 250- μ m-long EO phase shifter with waveguide cross-section dimension of 430×220 nm². Both of the arms are integrated with lateral-junction p-i-n diodes on rib-type Si waveguides, whose doping concentration is $\sim 10^{20}$ cm⁻³ [12]. All MZIs are driven by external digital-to-analog converters (DACs) connected to EO phase shifters.

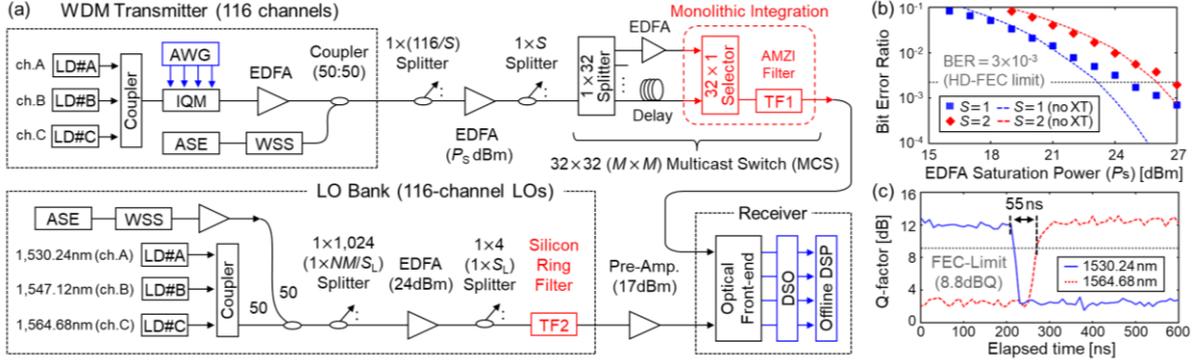


Fig. 4: (a) Experimental setup of $3,714 \times 3,714$ optical switch with 32-Gbaud DP-QPSK signals ($M = 32$, $N = 116$, and $S_L = 4$). (b) Measured BERs against EDFA saturation powers (P_s) with and without crosstalk (XT). (c) Switching response of Q-factors.

Figs. 3(c) and 3(d) show photographs of the fabricated chip and module, respectively. The footprint of the 32×1 space switch is 10×13 mm², including the PSRs inside the chip for on-chip polarization diversity. In the 35 nm wavelength range, the average fibre-to-fibre insertion loss and PDL were ~ 22 dB and < 1.5 dB, respectively. As depicted in Fig. 3(e), we performed time-resolved transmittance measurements by simultaneously changing the optical path from input port 11 to input port 12 and the filter passband centre from 1530 nm to 1565 nm. The switching time was shorter than 50 ns even though the time delay induced by DAC's response is included. The delay will be minimized if we employ high-speed drivers for carrier injection to EO phase shifters [16]. Fig. 3(f) shows the response time when one MZI switch element was driven by a 4-channel pulse generator. The result, which records 8-ns transition time for 90% power level transition, matched our analysis (Fig. 2).

Experiments

Fig. 4(a) presents the setup of our experimental $3,712 \times 3,712$ optical switch with fabricated 32×1 space switch. The transmitter generated 3-channel 32-Gbaud DP-QPSK signals using three LDs and a dual-polarization IQ modulator (IQM) driven by an arbitrary waveform generator (AWG). Their wavelengths were set at 1,530.24 nm (Ch.A), 1547.12 nm (Ch.B), and 1,564.68 nm (Ch.C) to replicate the edge and centre channels of the C-band. We emulated 116-ch. \times 128-Gb/s DP-QPSK signals (37.5-GHz grid) by combining 113-channel spectrally-shaped ASE (SS-ASE) lights obtained by using a wavelength selective switch (WSS) as dummy channels. The resultant WDM signal was divided by a $1 \times (116/S)$ splitter, then amplified by an EDFA with saturation power of P_s , and then distributed by a $1 \times S$ splitter. The 32×32 MCS created two copies of the signal with controlled amplitude and different symbol delay using a 1×32 splitter to emulate crosstalk (XT) of -15 dB (total). One of the two paths was

selected and then filtered by the fabricated module consisting of a 32×1 selector and TF1. In an LO bank, 37.5-GHz-spaced 116 LO channels were emulated by multiplexing three LD lights with an SS-ASE light. The multiwavelength light was broadcasted by cascaded two-stage splitters ($1 \times 1,024$ and 1×4 splitters), with an EDFA inserted after the first splitter to maintain the output power of 24 dBm. One target wavelength channel was extracted by the silicon ring filter (TF2) [17] and amplified to 17 dBm via a preamplifier prior to the receiver. The beat of the signal and LO was detected with an optical front-end, digitized using a digital storage oscilloscope (DSO), and passed through offline digital signal processing (DSP).

We measured bit error ratios (BERs) on the central channel (Ch. B) and compared performance without crosstalk where EDFA saturation power (P_s) was changed as per Fig. 4(b). With a crosstalk penalty of ~ 1.5 dB, the necessary saturation powers were found to be 24 dBm and 27dBm at the HD-FEC limit ($BER = 3 \times 10^{-3}$) for $S = 1$ and 2, respectively. We expect that the required saturation powers can be greatly reduced by reducing fibre-to-chip coupling loss [18]. Fig. 4(c) plots measured Q-variations over elapsed time when the signal switches from input port 1 to port 32 and from Ch. A to Ch. C. The LO wavelength was fixed to evaluate just the switching speed of the fabricated MCS. We achieved a fast switching time of 55 ns using trained DSP parameters, which matches the power-transient measurements [Fig. 3(e)]. The time can be reduced further by using a high-speed voltage driver.

Conclusions

We fabricated an EO Silicon-Photonic circuit for creating fast and high-port-count optical switches. The fibre-to-fibre loss can be improved by about 5 dB, which can enhance EDFA sharing by 3.2 times. The obtained switching time, 55 ns, corresponds to the round-trip-time of 5.5-m fibre, and basically does not impact average connection set-up latency in a DC floor span (e.g., 100 m).

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