50 Gbps Vertical Separate Absorption Charge Multiplication Ge/Si Avalanche Waveguide Photodetectors Integrated in a 300-mm Si Photonics Platform

Artemisia Tsiara[(1),*,**], Mathias Berciano[(1),**], Didit Yudistira[(1)], Roger Loo[(1)], Solomon Musibau[(1), (2)], Peter Verheyen[(1)], Filippo Ferraro[(1)], Yoojin Ban[(1)], Kristof Croes[(1)], Joris Van Campenhout[(1)]

[(1)] imec, Kapeldreef 75, 3001 Leuven, Belgium, *artemisia.tsiara@imec.be **both authors contributed equally
[(2)] KU Leuven, Department of Materials Engineering, Kasteelpark Arenberg 44, 3001 Leuven, Belgium

Abstract *We report 35 GHz Ge-on-Si avalanche photodetectors integrated on 300-mm SOI wafers, enabling high-quality eye diagrams at 50 Gbps NRZ, and low thermal drift of the breakdown voltage (<9 mV/°C). Early stress tests show only a mild drift of dark current and breakdown voltage.*

Introduction

Silicon Photonics (SiPho) technology has been gaining momentum in recent years as a solution for the increasing demand for high-speed data transmission at low-power consumption in datacenter and high-performance computing networks [1]. At the receiver side, germanium (Ge) photodetectors have been the workhorse of silicon photonics integrated circuits (PICs) for many years, leveraging the material's compatibility with the existing complementary metal oxide semiconductor (CMOS) platforms and its capability to detect light in the infrared (IR) region. However, traditional, p-i-n photodetectors provide insufficient receiver sensitivity when targeting a larger optical link budget, and this is where Avalanche Photodetectors (APDs) can provide a solution.

One of the most effective APD architectures is the Separate Absorption Charge Multiplication (SACM) APD [3], [4]. Waveguide-coupled Ge-on-Si SACM APDs have been developed in two configurations: Lateral and Vertical [4]–[7]. From a reliability point-of-view, a key point of attention are the misfits and threading dislocations formed in Ge during the direct growth of Ge on Si, due to the 4.2% lattice mismatch between the two materials. These defects can increase the dark current (I_{dark}) of the APDs, compromising the desirable Signal-to-Noise Ratio (SNR) [8]. Also, since the APDs require high bias voltages to operate, the generated high electric field could impact the dark current as well. In addition, these components are sensitive to temperature variations and the main parameters such as the breakdown voltage (V_{br}) or the gain could be impacted. Even though there are several publications reporting package-level stress tests [9]–[11], they only focus on the pass/fail result.

In this paper, we report a detailed study on the wafer-scale performance, temperature sensitivity and early reliability assessment of waveguide 50 Gbps-NRZ capable VSACM APDs, fully integrated in a 300-mm SiPho platform, along with other Si devices such as high-performance ring modulators [12], [13] and low-loss WDM filters [14].

Device design and fabrication

The VSACM APDs were fabricated in imec's 300-mm CMOS pilot line [15], using Silicon-On-Insulator (SOI) wafers with a 220 nm top Si layer on a 2 µm thick Buried Oxide. The multiplication layer is implemented in a 250 nm thick silicon epitaxial layer, deposited using Selective Epitaxial Growth (SEG) in a patterned oxide layer. The charge layer is defined by a low energy and low dose Boron-based implant in this layer, followed by the epitaxial growth of a 400 nm thick germanium layer, and p-type ion implantation for the top contact. Finally, tungsten contact plugs and Cu metal lines were formed on the Si and Ge layers contact regions. A detailed cross-section is shown in Fig. 1. The device dimensions in the Design of Experiments (DoE) consists of a 2 µm wide and 5/10/15 µm long Ge waveguides.

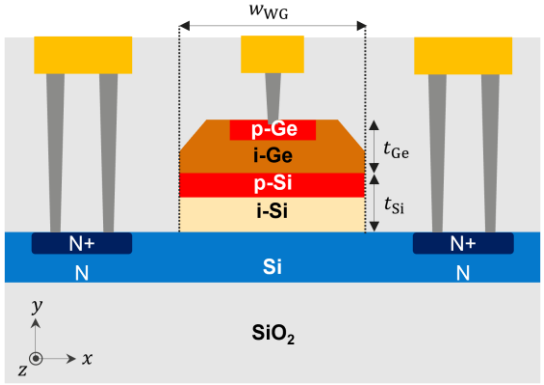

Fig. 1: Cross-section of the waveguide coupled vertical SACM avalanche photodetector.

Optoelectrical characterization

First, the optoelectrical performance of the APDs

in the O-band (1310 nm) was evaluated by dark and light current-voltage (I-V) DC sweeps and S-parameters RF characterization up to 50 GHz (Fig. 3), to extract I_{dark}, responsivity, gain, and the 3-dB bandwidth.

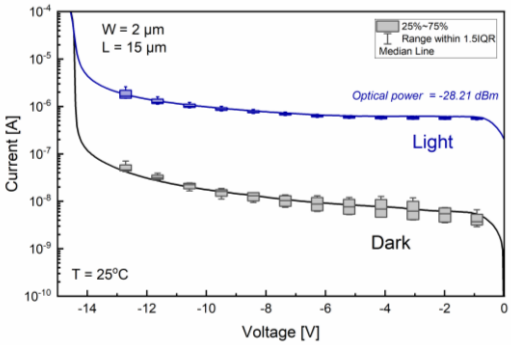

Fig. 2: Dark and light I-V characteristics of the 15 µm long Ge/Si VSACM APD (N_{dies}=5, λ=1310 nm).

Measured APD I-V curves from multiple dies demonstrate a sharp avalanche breakdown for lower voltages than -14 V (Fig. 2). The APD breakdown voltage is defined when the current reaches 10 µA, while the dark current is calculated at 90% of the breakdown voltage, yielding typical values of < 150 nA at room temperature.

The primary responsivity is measured to be 0.5 A/W at 1310 nm. At a bias of -13 V, the extracted bandwidth is 35 GHz, and gain M=4, for a responsivity of 2 A/W (Fig. 3). At lower gain values, bandwidths up to 50 GHz can be obtained.

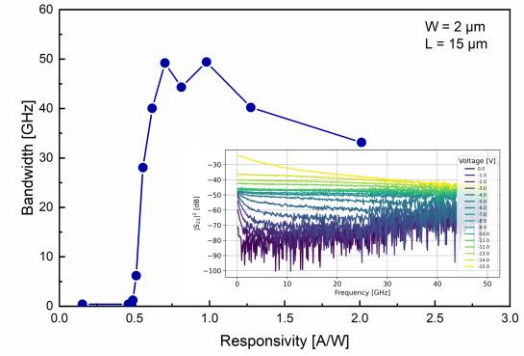

Fig. 3: 3-dB bandwidth versus responsivity of the 15 µm long Ge/Si VSACM APD, operating at 1310 nm. Inset refers to S_{21} measurement data for different applied bias voltages.

Next, the large signal response of the APDs was evaluated by measuring on-wafer eye diagrams, using an external reference modulator (35 GHz, ER=13 dB) driven by a pseudorandom binary sequence with pattern length of 2^{31} -1 (PRBS31) at 50 Gbps NRZ data rates (Fig. 4). At -13 V bias (M=4), a Signal-to-Noise Ratio (SNR) of 6.1 was extracted, illustrating the capability of the APD to operate at 50 Gbps NRZ lane rates with high signal quality, and 2-3x higher responsivity than best-in-class Ge/Si p-i-n PDs, while retaining low dark currents. Improved gain and bandwidth performance is expected with further optimization of the doping profiles of the VSACM structure.

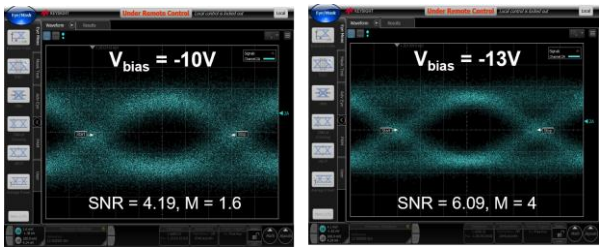

Fig. 4: On-wafer eye-diagrams at 50 Gbps of the APD for different bias voltages and gain (NRZ-OOK, PRBS31).

Temperature sensitivity

Subsequently, the temperature-dependence and origin of the dark current of the as-fabricated devices has been analyzed, by performing I-V sweeps, from 25 °C up to 100 °C, keeping the current compliance at 10 µA (Fig. 5).

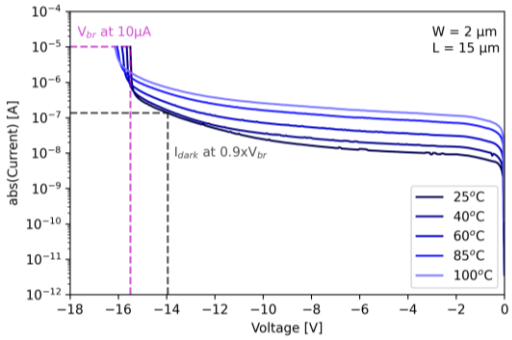

Fig. 5: Typical dark current versus bias voltages for different temperatures.

Performing a linear fit of the V_{br} values with respect to temperature, the temperature coefficient (T_{coeff}) of the breakdown voltage was deducted. Fig. 6 summarizes the values for the smallest geometry (width and length), confirming the low temperature sensitivity (less than 9 mV/°C) of the APDs, characteristic of Ge/Si APDs with narrow multiplication region [16].

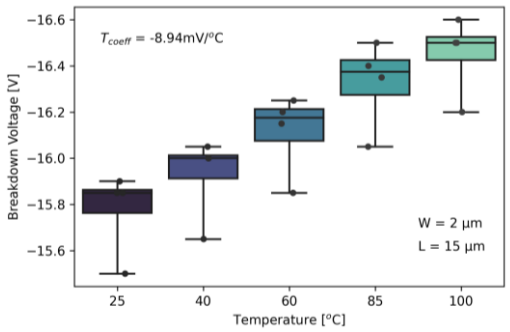

Fig. 6: Temperature coefficient of the APD breakdown voltage, showing low temperature sensitivity (< 9 mV/°C).

The activation energy (E_A) is determined by the Arrhenius relationship, $|I| \propto \exp(-E_A/k_BT)$, with k_B as the Boltzmann constant and T as the

absolute temperature. The extracted activation energy at different reverse voltages (Fig. 7) shows a clear electric field dependence for all tested design variations. Up to -8 V of reverse bias, the extracted E_A is 0.33eV, half the bandgap (E_g/2) of Ge, pointing to a Shockley-Read-Hall (SRH) process. As the reverse bias increases, and thus the depletion region is extending towards the Si, there is a decrease of the activation energy. This indicates a change in the conduction mechanism towards Trap-Assisted-Tunneling (TAT), reported also previously for Ge p-i-n PDs [17], with the defects at the Ge/Si interface being the suspected root cause. Overlapping the experimental data with TCAD simulations (Fig. 7&8), there is a good agreement for the high bias regime, while the mismatch in the low bias region can be improved by tuning the recombination parameters of the Ge layer.

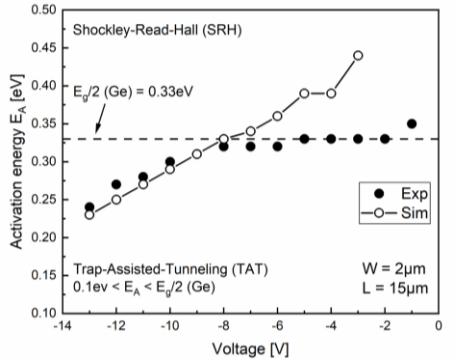

Fig. 7: Simulated and measured activation energy E_A values indicate a change of the conduction mechanism from low (SRH) to high reverse bias (TAT).

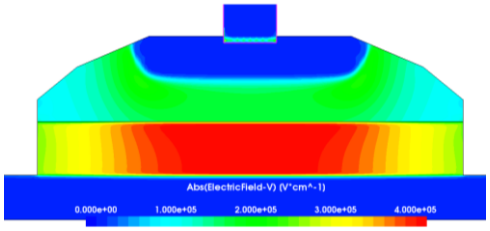

Fig. 8: Simulated electric field values at V_{bias} = -13 V of ~400 kV/cm at the Ge/Si interface suggest that defects in this region are a root cause for TAT.

Early reliability assessment

The degradation kinetics of the APDs were studied through accelerating ageing (standard Measure-Stress-Measure (MSM) technique) under a constant reverse current of 100 µA and for a total stress time of 5000 s, monitoring the shift of the device parameters at various stress temperatures up to 150 °C. The temperature was kept constant during the stress and characterization phases, with 3 dies tested per condition. The median of them is shown in Fig. 9.

Calculating the maximum relative V_{br} shift (Fig. 9a) for the entire DoE, demonstrates less than 7% drift for an operation up to 100 °C.

A second important parameter of the avalanche photodetectors is the dark current. The max relative I_{dark} shift as shown in Fig. 9b, for one length (L_{WG}=15 µm) and one width (w_{WG}=2 µm) combination, decreases for the reported tested conditions, with no temperature dependence. This behaviour can be attributed to a more pronounced trapping of the generated charges in the depletion region that extends as the bias increases from -2 V (bulk Ge) to -12 V (Ge/Si interface), potentially originating from additional electric field due to corner effects. Similar results are collected for the two additional lengths.

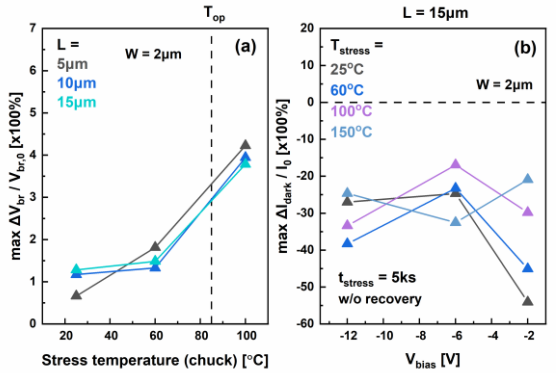

Fig. 9: (a) Max relative V_{BR} shift for all tested T_{stress}, and (b) max relative I_{dark} shift w.r.t. V_{bias} for different stress conditions, both indicating potentially beneficial impact of a narrow width device.

Conclusions

We presented the performance and early reliability study of 50 Gbps-capable waveguide VSACM avalanche photodetectors, integrated in a 300-mm SiPho platform. A bandwidth of 35 GHz at 2 A/W responsivity was demonstrated at 1310 nm wavelength, along with dark currents below 150 nA, across the wafer. A low temperature sensitivity of the breakdown voltage was achieved (< 9 mV/°C). In initial electrical stress tests, a mild decrease in dark current, and a mild increase of the V_{br} (< 7%) were observed, providing a positive outlook towards enabling thermally robust and reliable APD devices for optical interconnects in future datacenter and HPC systems.

Acknowledgements

This work was supported by imec's industrial affiliation R&D program on Optical I/O and the European Commission via the H2020 project SiPho-G (101017194). The authors would like to thank Rafał Magdziak and Hakim Kobbi for performing DC and RF optoelectrical measurements, respectively. Special thanks to Ints Murãns for measuring the eye diagrams.

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