

# Ultra-High-Symbol-Rate Optical Transceivers

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**Abstract** We discuss the possible techniques for future ultra-high symbol rate optical transceivers. ©2023 The Author(s)

## Introduction

Optical transceivers are one of the fundamental building blocks for fiber communication systems. In the past ~1.5 decades, the throughput of deployed long-haul fibers has increased from several Tb/s/fiber to ~40 Tb/s/fiber [1]. In terms of lab demonstrations, the record per fiber throughput for long-haul distance has increased from ~20 Tb/s to ~70 Tb/s [2]. Such improvement is largely due to the advances in optical transceivers. Around 2010 when coherent technology starts to be widely deployed in the field, the optical transceivers operate at ~30 GBaud and carries 100 Gb/s per wavelength. Now, a commercial coherent transceiver operates at ~130 GBaud and carries up to 1.2 Tb/s per wavelength [3]. The data rate per optical transceiver has significantly increased thanks to the progress we made on complementary metal-oxide-semiconductor (CMOS) technologies, advanced digital signal processing (DSP), and higher bandwidth analog components such as modulators, photodiodes, and electrical drivers.

The future of high-speed fiber transmission still relies on the further development of optical transceivers. In this paper, we discuss the possible techniques for future high-speed optical transceivers.

## Ultra-high-speed components for optical transceivers

We have been observing ~60% annual traffic growth for the past several decades [1]. Meanwhile, the interface rate of an optical transceiver has been increasing at a steady pace of only ~20% per year. Such an increase is attributed to the advances in the development of many of the key components in optical transceivers. For instance, optical modulators become much smaller and more efficient [4-12]. The 100 Gb/s coherent transmitters use traditional LiNbO<sub>3</sub> modulators which are typically ~8-cm long with a half-wave voltage  $V_{\pi}$  of ~3.5 V and 3-dB bandwidth of ~35 GHz [4]. The current generation commercial transceivers typically use silicon photonic (SiPh) or indium phosphide (InP). SiPh modulators have similar 3-dB bandwidth compared to traditional LiNbO<sub>3</sub>

ones but significantly smaller sizes [5]. InP modulators can have higher speeds than traditional LiNbO<sub>3</sub> modulators, with only a slightly larger form factor compared to SiPh ones [6]. Besides the technologies that are made into products, some technologies under research show great potential for scaling to even higher bandwidth. For example, thin-film LiNbO<sub>3</sub> (TFLN) modulators offer 100-GHz bandwidth supporting 200-GBaud signals with < 2 V driving voltage [7-9]. The plasmonic modulators can have an extremely small size of only ~20  $\mu\text{m}$  and an ultra-high 3-dB bandwidth of ~500 GHz, although they are lossier and require higher  $V_{\pi}$  [10]. Another type of new modulator, the silicon-organic hybrid (SOH) modulator, also features a small size (< 1 mm) and low  $V_{\pi}$  (< 1 V) [11]. The stability of the organic material is still under investigation.

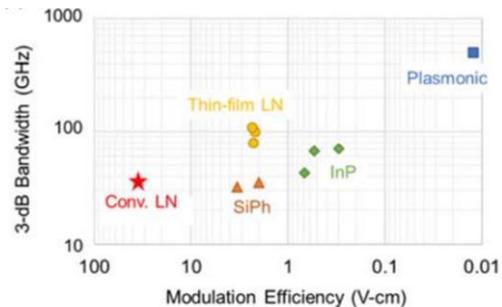


Fig. 1 Comparison of MZM's 3-dB bandwidth and modulation efficiency (some of the technologies are not shown in this figure as the 3-dB bandwidths were not reported).

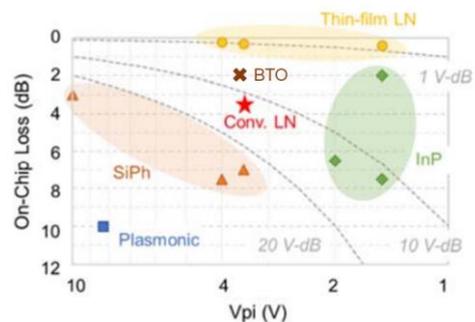


Fig. 2 Comparison of device loss and the required driving voltage ( $V_{\pi}$ ).

Figure 1 shows a comparison of some new modulators' bandwidths and modulation efficiencies. The modulation efficiency is defined

as the product of  $V_{\pi}$  and its length (the smaller product, the better). The conventional  $\text{LiNbO}_3$  modulator (marked as a red star) is plotted as a reference. We can see that the new modulators not only have much better modulation efficiency but also significantly higher bandwidth. The other important aspect of modulators is device insertion loss. Figure 2 shows a comparison of on-chip loss as a function of driving voltage. We can see that both thin-film  $\text{LiNbO}_3$  and InP modulators are less lossy than the conventional  $\text{LiNbO}_3$  ones.

### Integrated CMOS and external multiplexing

While the analog parts (modulators, photodiodes, RF amplifiers, etc.) are going relatively strong in terms of scaling up in the bandwidth, the CMOS-based application-specific integrated circuit (ASIC) for the DSP is one of the major reasons why the transceiver speed is increasing at a limited pace. The first-generation ASIC for coherent optical transceivers was based on 65-nm CMOS, allowing ~30 GBaud electrical signal generation. In 2023, optical transceivers are equipped with 5-nm CMOS supporting ~130 GBaud signal generation. This reflects only a ~13% symbol rate increase per year. Furthermore, it is predicted that the CMOS speed may saturate once the node size becomes too small. This means even the 13% symbol rate increase may not be maintained in the long term.

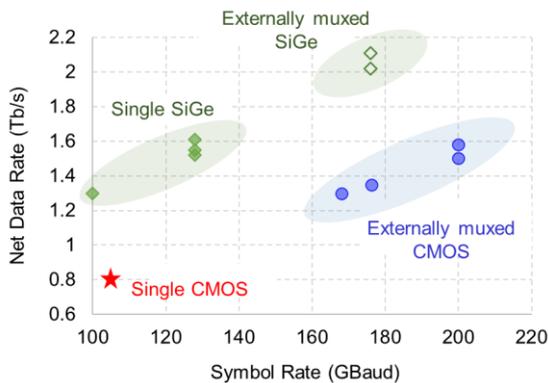


Fig.3 Lab demonstrated high-symbol-rate coherent systems.

As CMOS remains the most suitable platform for DSP, externally multiplexing CMOS-generated analog signals can potentially be a good option. Lab demonstrations have shown that multiplexing two or more CMOS signals can result in 222-GBaud binary signals and up to 200-GBaud multi-level signals [13 - 16]. Figure 3 shows an overview of the lab-demonstrated high-symbol-rate single-wavelength systems. As shown, the highest data rates from CMOS systems are implemented with external DAC multiplexing. We can also see that SiGe DACs achieve higher speeds than CMOS, but at the

moment it is not clear how the SiGe DACs can be integrated with the CMOS-based DSP.

### Digital band interleaved (DBI) DAC and high symbol rate transmission

DBI-DAC is one of the ways to implement external DAC multiplexing [14]. An exemplary diagram of a DBI-DAC is shown in Fig.4. This is an illustration of a DBI-DAC aiming for generating 100-GHz bandwidth electrical signals which support up to 200 GBaud signals. The 100-GHz bandwidth signal to be generated is first digitally cut into three spectral slices in the DSP unit. Each spectral slice occupies ~35 GHz bandwidth and is then treated as a baseband signal and is converted to an analog signal using its own baseband DAC (DAC1, 2, and 3 in Fig. 4). A fourth DAC (DAC4) is used to generate local oscillator (LO) seed tones (one at ~17 GHz and the other at ~13 GHz). All four DACs are on a common CMOS chip and share the same clock source, therefore they are synchronized. These two seed frequencies will then be upconverted to ~68-GHz and ~104-GHz respectively, via frequency multipliers. The up-converted sinusoidal waves will then act as electrical LOs. After the baseband signals are upconverted to their corresponding frequencies, a triplexer is used to combine the three bands. A calibration is then done to measure the power and phase/delay differences among the three bands, and a pre-compensation is applied to remove the associated distortion. More details of the principles of DBI-DACs can be found in Ref.14.

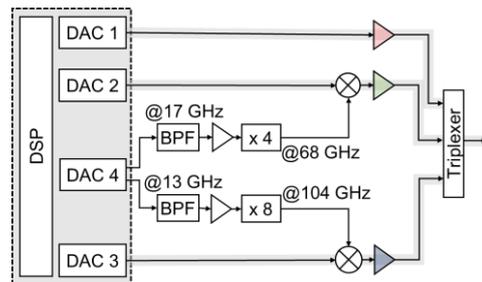


Fig.4 Exemplary schematic of one method to implement a 100-GHz DBI-DAC (BPF: band-pass filter).

A unique advantage of such a band interleaving technique, compared to other multiplexing techniques like analog multiplexer (AMUX, as shown in e.g. Ref.15 or 13), is that there is no need to design a broadband driver/amplifier for the 200-GBaud signal. The three frequency bands can be individually amplified with banded drivers, which is easier to design/fabricate compared to a broadband (DC – 100 GHz) amplifier.

We build a DBI-DAC that has 102-GHz bandwidth and generates up to 200-GBaud electrical signal. We then modulate this signal onto the optical domain using a 100-GHz TFLN

modulator. We first use a Mach-Zehnder modulator (MZM) and demonstrate an intensity modulation and direct detection (IM-DD) system [17]. The optical transmitter consists of one external cavity laser (ECL), a DBI-DAC, and a TFLN MZM. The modulator is biased at its quadrature point for intensity modulation. The optical signal is then amplified and transmitted through a 10.2-km standard single-mode fiber (SSMF), followed by dispersion compensation fiber (DCF). The receiver consists of a 100-GHz single-ended photodiode and a 113-GHz real-time scope. A detailed description of the experimental setup can be found in Ref.17. The recovered eye diagram and histogram are shown in Fig.5 (a) and (b). An example of the received digital spectrum is shown Fig. 5 (c). We use probabilistically shaped (PS) PAM-16 and entropy loading to maximize the data rate. The recovered constellation signal-to-noise ratio (SNR) for single carrier PS-PAM-16 is 17.0 dB, and the achieved net data rate for the 200-GBaud single carrier signal is 484.5 GB/s. The achieved net data rate with entropy loading is 538.8 Gb/s.

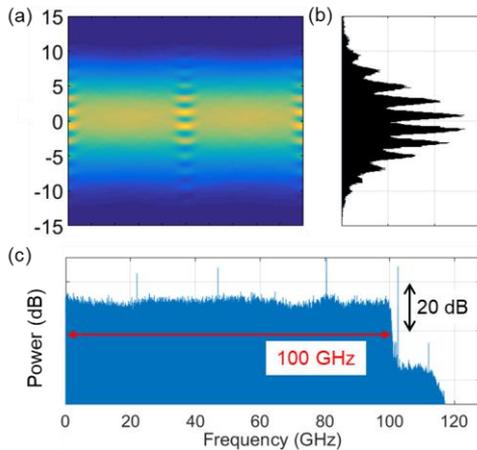


Fig.5 (a) and (b) Received eye diagram and histogram of the 200-GBaud PS-PAM16 IM-DD signals with 10.2-km fiber transmission; (c) received digital spectrum.

After the IM-DD experiment, we then construct two of the DBI-DACs and use a TFLN I/Q modulator to form a 200-GBaud coherent system. Two independent DBI-DACs are used for the I and Q part of the coherent signals. A single polarization TFLN I/Q modulator is used for E/O conversion, followed by polarization emulation. A dual-polarization 100-GHz coherent receiver is used to receive the signal after 21-km SSMF transmission. More details of the experimental setup can be found in Ref.18. The received digital spectrum of the 200-GBd PS-64-QAM signal after transmission is shown in Fig.6 (b). The recovered constellations are shown in Fig.6 (a). The recovered constellation SNR at the optical back-to-back setting is 13.6 dB, and the resulting net data rate is 1.58 Tb/s. After the 21-km

transmission, the SNR decreases slightly to 13.2 dB, and the net data rate becomes 1.50 Tb/s.

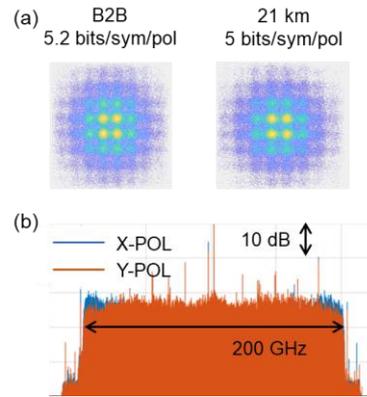


Fig.6 (a) Recovered constellations of 200-GBaud PS-64-QAM coherent signal at optical back-to-back and after 21-km SSMF transmission; (b) the received digital spectrum of the 200-GBd signal.

## Summary

The improvement made from higher speed hardware as well as electrical multiplexing can increase the interface rate by several times. However, unlikely these will be enough to sustain the continuing 60% annual traffic growth. With other physical dimensions such as quadrature and polarization fully explored, we are left with the single remaining dimension which is space. This led to the very active research topic of space-division multiplexing (SDM). For transceivers, multiplexing in space means parallel transceivers in one package. Assuming the 60% traffic growth continues (as little evidence predicts otherwise), we can expect 100x traffic increase in 10 years. With the ~20% increase per transceiver speed, we will need to integrate > 20 transceivers into a module in the future. The close integration of multiple transceivers opens the opportunity to globally optimize the design of DSP, RF components, and optics across transmitters/receivers. Problems that may be difficult or resource-costly to solve in hardware design may be solved in DSP with minimal additional complexity. One example is that one can allow crosstalk among modulator electrodes to save space but pre-compensate such crosstalk in transmitter DSP [19]. It will also be possible to optimize e.g. the modulation formats and the number of transceivers to achieve the optimal balance among cost, form factor, and power consumption.

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