Large-Scale Silicon Photonic MEMS Switch with Flip-Chip Integrated CMOS Drivers

Johannes Henriksson[1,*], Erik Anderson[1], Kyungmok Kwon[1], Jianheng Luo[1], Vladimir Stojanović[1], and Ming C. Wu[1]

[1] Department of Electrical Engineering and Computer Sciences; UC Berkeley, CA, USA
*Author email address: jhenriksson@berkeley.edu

Abstract *We report on 32x32 silicon photonic switches controlled by digital CMOS chiplets with integrated high voltage drivers. Digital switching with sub-microsecond switching speed and 97 mW power consumption is experimentally demonstrated. ©2023 The Author(s)*

Introduction

As the data rates inside datacenters and supercomputers continuously grow, increased attention is given to how future scaling and performance gains can be secured while simultaneously maintaining reasonable power consumption.

Recently, Google announced large-scale deployment of optical circuit switches (OCSes) in its datacenter networks, eliminating electrical package switch-based spine blocks to enable flexible topology engineering, improved intra-datacenter expansion and rapid technology refresh [1]. OCS were also integrated into supercomputer networks specific for machine learning, where the ability to dynamically reconfigure the topology improves scaling, power consumption, utilization and performance [2].

While Google uses 3D MEMS optical switches, a technology based on free-space optics with millisecond-order switching time, much work has been done in recent years in the field of integrated optical switches. Silicon photonics (SiPh) fabrication process leverages the mature complementary metal-oxide-semiconductor (CMOS) technology with potential to deliver higher density, lower-cost, more energy efficient and faster optical switches.

Often, SiPh switch architectures rely on cascaded 2x2 Mach-Zehnder interferometer switch units, however, maintaining a low cumulative optical loss for such switch architectures has proved to be challenging – especially when scaling to high radices as outlined in [3].

Our group has previously reported on highly scalable, SiPh switches based on microelectromechanical-system (MEMS) actuators with sub-microsecond switching speed. Among our previous work is a 240x240 switch with 9.8 dB maximum on-chip loss [4], the largest integrated optical switch reported to date.

In this paper we, for the first time, demonstrate integration of high-voltage CMOS drivers with the SiPh MEMS switch using thermocompression flip-chip bonding.

Our integrated OCS exhibits at least 3 orders of magnitude faster switching time compared to 3D MEMS OCS [1,2]. It therefore opens the door for OCS deployment in new areas of network hierarchies that are not accessible for OCS technology available commercially today.

Additionally, while the 3D MEMS switch requires rigorous calibration due to the analog nature of its MEMS actuators, the SiPh switch presented here uses digital MEMS actuators and it thus vastly simplifies control, CMOS integration and eliminates the need for driver calibration.

Moreover, 3D MEMS actuators require 100s of volts whilst we can drive our SiPh MEMS actuators at approximately 50 V, a major difference that could enable more reliable, power and cost efficient OCS drivers in the future.

Switch Architecture and Design

Fig. 1 depicts the crossbar switch architecture used in this work. Orthogonal, low-loss, rib waveguides form a bus waveguide layer. On top of the bus layer is a second layer consisting of coupler waveguides.

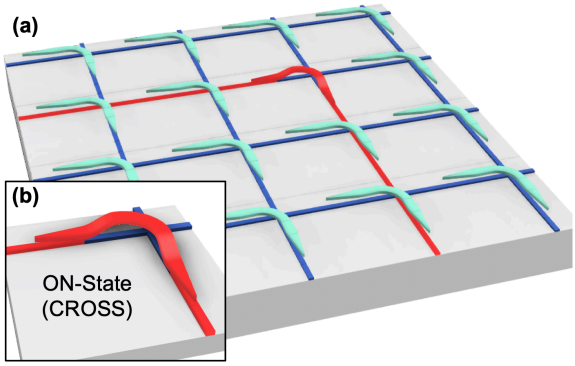

Fig. 1: (a) Rendering of a 4x4 optical switch. (b) Zoomed-in rendering of a switch unit cell in the ON-state.

When a switch unit cell is in its OFF-state (BAR), light travels straight through the bus waveguide with minimal optical loss. In the ON-state (CROSS), MEMS actuators bring adiabatic coupler waveguides into close proximity of the bus waveguides, allowing light to couple from one bus waveguide, through the coupler waveguide and into another bus waveguide.

Because of the switch's low-loss OFF-state and because every optical path only ever passes through exactly one ON-state switch unit cell, this architecture is highly scalable and is particularly desirable for large-radix integrated OCS.

In the work presented here, a 128x128 O-band silicon photonic switch was designed and fabricated. To support flip-chip bonding of multiple small-sized CMOS chiplets, the switch is divided into 16 blocks, each consisting of 32x32 switch arrays, see Fig. 2(a).

The footprint of a switch unit cell was set to 127 x 127 μm^2. This matches to the 127 µm pitch of the fiber array units (FAUs) used for optical I/O coupling. The electrodes of each switch unit cell's MEMS actuator are connected to two pads within the switch unit cell, enabling the CMOS chiplet to interface directly to each of the 32^2 switch unit cells.

The SiPh MEMS process is based on 220 nm silicon-on-isolator with 60 nm partially etched bus waveguides. A 300 nm thick poly-silicon film with 200 nm partial etch make up the MEMS actuator and coupler waveguide layers. A more detailed description of the fabrication process, optical and MEMS design can be found in [4] and [5].

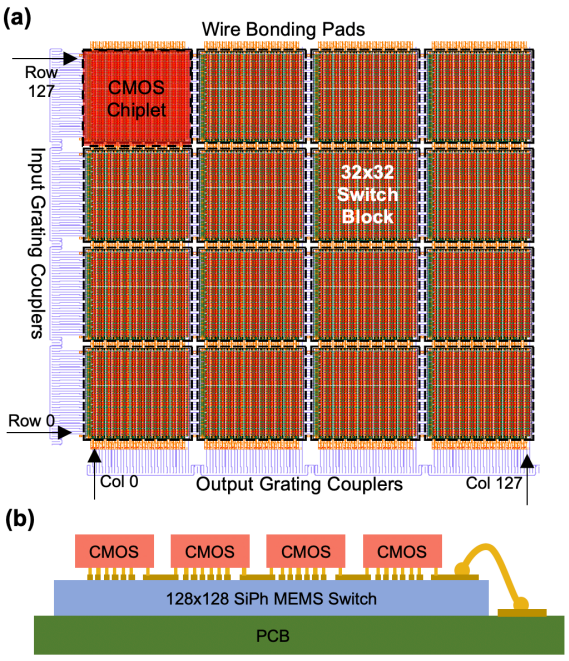

Fig. 2: (a) Layout of 128x128 switch with single CMOS chiplet bonding location marked for 32x32 package. (b) Schematic of electrical connections between CMOS chiplets, SiPh chip and PCB.

CMOS Design and Integration

To provide the SiPh MEMS switch with electrical control and a digital interface, a high-voltage application-specific integrated circuit (ASIC) chiplet was designed and fabricated. Each CMOS chiplet contains 1024 high-voltage, digitally controlled, level shifters – enabling the chiplet to control a 32x32 switch array. To minimize the switch control serialization latency, each chiplet has 8 parallel scan-chains, each controlling 4 columns.

The CMOS drivers can support a maximum of 70 V bias to the MEMS actuators. This far exceeds the minimum MEMS turn-on voltage of 41 V, which can be extracted from Fig. 4(f). This figure also shows the digital characteristics of the MEMS actuators and the excellent extinction ratio between ON and OFF state.

If the CMOS chiplets are bonded in a 4x4 array, then the full 128x128 SiPh MEMS switch can be controlled. In such configuration, CMOS chiplets in a given column are connected in series through the SiPh chip. The SiPh chip is, in turn, connected to a PCB via wire bonds, see Fig. 2(b).

The CMOS chiplets were fabricated in TSMC's 180nm HV BCD Gen 2 process. During post-processing, under-bump metallization (UBM) and gold cylinder-shaped nano-shell bumps were added on both CMOS and MEMS. We used thermocompression bonding which, because it is a dry process, is compatible exposed waveguides and MEMS actuators.

Experimental Result

A single CMOS chiplet was bonded to a 128x128 SiPh switch chip, effectively making it a 32x32 switch package and demonstrating successful integration of CMOS drivers with SiPh MEMS switches. Packaging of the full 128x128 switch chip is left as future work.

To fully characterize all 32^2=1024 possible optical paths through the silicon photonic switch, an automated test setup was built. Light is coupled between fibers and on-chip bus waveguides using grating couplers and two 72-channel FAUs, see Fig. 3(a). The FAUs are connected to two 1x64 OCS, one of which is connected to, through a motorized polarization controller, a tunable O-band laser. The other 1x64 OCS connects to a low-noise optical power meter and a high-speed photodiode. The CMOS driver chiplet is controlled by a field-programmable gate array (FPGA).

With this setup we can input light into any of

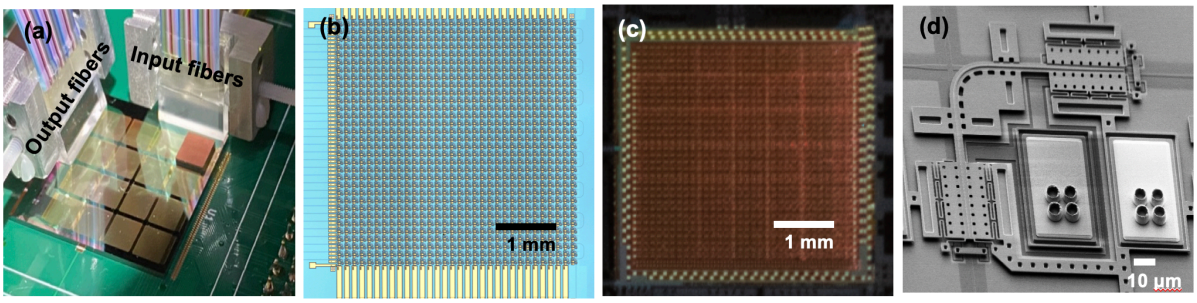

Fig. 3: (a) A single CMOS chiplet bonded to SiPh switch chip and aligned fiber array units. (b) Micrograph of 32x32 SiPh switch block. (c) Micrograph of CMOS chiplet. (d) SEM micrograph of switch unit cell including pads with Au nano-shell bumps.

the 32 input ports (rows), monitor light from any of the output ports (columns) and turn on any of the 32^2 MEMS actuators without needing to re-align any FAUs, reconnect any fibers or move electrical probes. Compared to our previous work on large-scale switches, this represents a significant improvement in testing capability.

Fig. 4(a) shows the measured on-chip loss at 1310 nm wavelength for each of the 32^2 possible optical paths through the switch array. As can be seen, only 3 switch unit cells were defect (white color), resulting in 99.7% yield.

High-loss columns and rows can clearly be identified from Fig. 4(a). We attribute the higher loss to a waveguide damage from testing and/or lossy fiber connections in the off-chip connections between FAUs and 1x64 OCS.

Because the CMOS chiplet was bonded to top-left corner of the 128x128 switch chip, each of the 32^2 characterized optical paths passes through 96 extra OFF-state switch unit cells and accumulate estimated 3.8 dB excess optical loss compared to a SiPh chip designed exclusively for 32x32 radix.

Using 60 V MEMS bias, the turn-ON and turn-OFF times were 0.81 µs and 0.44 µs respectively. As can be seen Fig. 4(b)(c)(e), the switching time uniformity is excellent with all non-defect switch unit cells switching in less than 1 µs. Thus, CMOS and SiPh MEMS can be integrated with great uniformity.

Using 60 V MEMS bias, 50 MHz CMOS clock frequency and 96 mW power, the 32x32 switch can be fully reconfigured every 0.58 µs (this number does not include the optical response delay shown in Fig. 4(e)).

Conclusions

In summary, we demonstrate integration between silicon photonic MEMS switches and high-voltage CMOS drivers. A 32x32 switch package is fully characterized; sub-microsecond switching times, 8.2 dB average on-chip loss and 97 mW power consumption.

Acknowledgements

This work was supported by the DARPA PIPES program and the ARPA-E ENLITENED program.

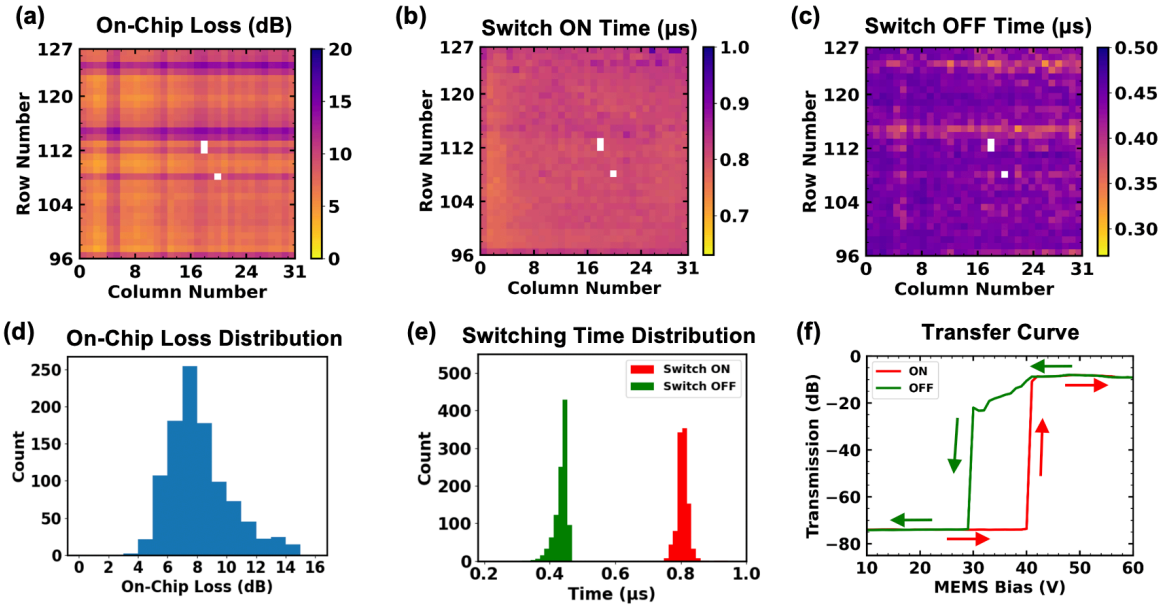

Fig. 4: Map of on-chip loss (a), switch-ON time (b) and switch-OFF time (c) for all 32^2 switch paths. (d) Same as (a), but in histogram form – with approximately 3.8 dB excess loss from 96 extra OFF switch unit cells. (e) Same as (b) and (c) but in histogram form. (f) Transfer curve for single switch unit cell.

References

[1] Urata, R., Liu, H., Yasumura, K., Mao, E., Berger, J., Zhou, X., Lam, C., Bannon, R., Hutchinson, D., Nelson, D. and Poutievski, L., 2022. Mission Apollo: Landing optical circuit switching at datacenter scale. *arXiv preprint.* DOI: 10.48550/arXiv.2208.10041.

[2] Jouppi, N.P., Kurian, G., Li, S., Ma, P., Nagarajan, R., Nai, L., Patil, N., Subramanian, S., Swing, A., Towles, B. and Young, C., 2023. Tpu v4: An optically reconfigurable supercomputer for machine learning with hardware support for embeddings. *arXiv preprint.* DOI: 10.48550/arXiv.2304.01433.

[3] Suzuki, K., Konoike, R., Suda, S., Matsuura, H., Namiki, S., Kawashima, H. and Ikeda, K., 2020. Low-loss, low-crosstalk, and large-scale optical switch based on silicon photonics. *Journal of Lightwave Technology*, *38*(2), pp.233-239. DOI: 10.1109/JLT.2019.2934768

[4] Seok, T.J., Kwon, K., Henriksson, J., Luo, J. and Wu, M.C., 2019. Wafer-scale silicon photonic switches beyond die size limit. *Optica*, *6*(4), pp.490-494. DOI: 10.1364/OPTICA.6.000490

[5] Seok, T.J., Quack, N., Han, S., Muller, R.S. and Wu, M.C., 2016. Large-scale broadband digital silicon photonic switches with vertical adiabatic couplers. *Optica*, *3*(1), pp.64-70. DOI: 10.1364/OPTICA.3.000064