Photonic Integrated Nanosecond 1×2 Wavelength Selective Switch On 3-μm Silicon Platform

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Abstract: *A 12-channel photonic integrated 1×2 electro-optic wavelength selective switch with nanosecond switching time is demonstrated on 3-μm silicon platform. Experimental results show 2.4ns switching time, 19.5dB average extinction-ratio, 7.8dB lowest insertion loss and error-free operation with <0.2dB power penalty at 10 Gb/s signal. ©2023 The Author(s)*

Introduction

Wavelength selective switch (WSS) is a key component in the reconfigurable optical add-drop multiplexer (OADM) system for flexibly routing any input signals to any output ports without electrical–optical–electrical conversion [1]. As many applications like 5G and beyond, edge-cloud service and internet of things as well as the network densification in metro-access networks, rapidly boost the volume of the data as well as the amount of OADM elements in metro-access networks and data center, low-cost WSS needs to be more stable and faster for efficiently managing the large, heterogeneous, and dynamic data traffic. The current commercial WSSs based on micro-electromechanical systems (MEMS) or liquid crystal on silicon (LCOS) technology have disadvantage of bulky size, high cost due to complex assembly and slow switching speed. Photonic integrated circuit (PIC) based WSSs are promising solutions with compact footprint, high stability, low cost, and low power consumption to implement fast programmable optical networks [2]. Many PIC-WSSs are realized on different photonic platforms with a configuration consisting of PIC Mux/Demux for the wavelength separation /combination and photonic switches/gates for wavelength bypass/dropping/blocking. In [3], a 1×2 PIC-WSS with arrayed waveguide grating (AWG) and Mach Zehnder Interferometer (MZI) switches on silica platform has 20 dB average extinction ratio, but large size of 60 mm × 78 mm and low switching speed due to thermo-optic effect. A 6-channel 1×2 thermos-optic PIC-WSS based on micro-ring resonators (MRRs) and 220-nm silicon platform [4] has compact size of 240 μm × 140 μm, but with milliseconds switching speed. A 1×1 wavelength blocker using variable optical attenuator as switching gate on 220-nm silicon platform [5] provides nanosecond operation and small size, but it has high insertion loss of 22 dB and low extinction ratio of 10 dB. A hybrid integrated WSS combining 3-μm silicon AWGs and InP semi-conductor optical amplifiers (SOAs) can provide nanosecond switching speed and high extinction ratio, but it currently presents high coupling loss between silicon waveguide and InP waveguide [6]. The 3-μm silicon photonic platform is the attractive option for achieving the monolithic integrated WSS with nanosecond switching, low insertion loss, high extinction ratio and low power consumption, since it provides low optical losses (~0.1 dB/cm), ultra-dense integration (μm-scale bend) [7] for compact AWG [8] and highly efficient electro-optic effect.

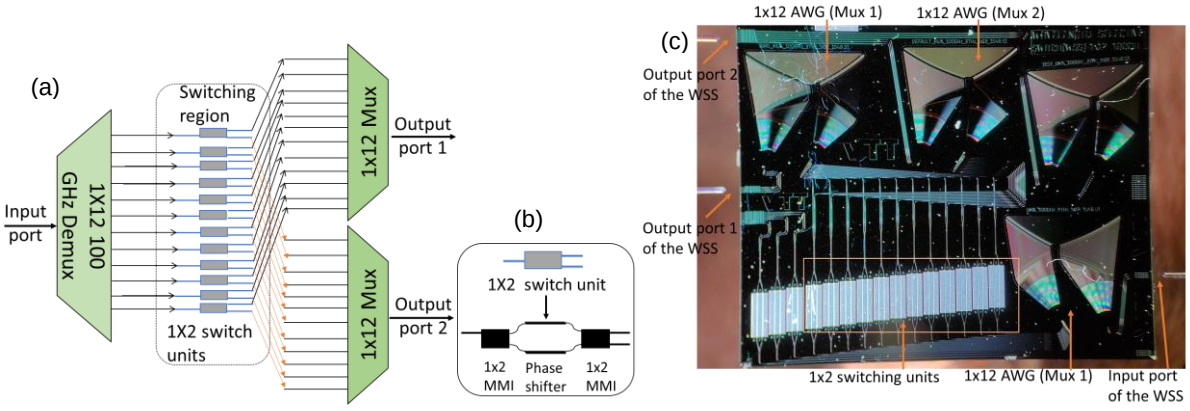

Fig. 1: (a) the configuration schematic of 1×2 WSS consisting of Demux/Mux and 1×2 switching units; (b) the structure of 1×2 MZI switching unit; (c) the micrograph of the 1×2 WSS chip.

Therefore the 3-μm silicon platform proving compact 100 GHz spacing AWG and fast switching unit based on plasma dispersion is a promising platform to implement a low-cost nanosecond 1x2 PIC-WSS.

In this paper, we demonstrate, for the first time to the best of our knowledge, a C-band 12-channels 100 GHz spaced 1×2 PIC-WSS on 3-μm silicon platform consisting of AWGs as Mux/Demux and 1×2 nanosecond switching units. Experimental results show that the 1×2 WSS has insertion losses ranging from 7.8 dB to 10.1 dB, 19.5 dB average extinction ratio between the two outputs, 4.2 ns switching rising time and 2.4 ns falling time. The device requires only 0.35 V switching voltage that results in 70 mW power consumption per channel. Transmission experiments show error free operation with < 0.2 dB power penalty at 10^{-9} BER for 10 Gbit/s data.

Design and fabrication of the 1×2 WSS

The 1×2 PIC-WSS design is shown in Fig. 1 (a). It includes three 12-channels 100 GHz spaced AWGs as Demux/Mux for separating/combining the WDM signals, 12 1×2 electro-optic switching elements to route the wavelengths to desired output port. The 1×12 100 GHz AWG employs directly 3 μm × 3 μm strip waveguide as the arrayed waveguide to have low insertion loss and low polarization dependent wavelength shift to effectively avoid the performance degradation caused by polarization variation in the PIC chip. The excitation of higher order modes in the strip waveguides is avoided by using adiabatic rib-strip converter. The single-mode rib waveguide is used for coupling light from the fiber to the chip with low loss. Also, the Euler bends based on strip waveguide enable ultra-dense integration and compact size (~ 6.6 mm^2) for 3-μm silicon 100 GHz spacing AWG. More details of the 1×12 100 GHz AWG building block is shown in [8]. The structure of the 1×2 MZI electro-optic switch is illustrated in Fig. 1 (b). It consists of a 1×2 multi-mode interferometer (MMI) as the input power splitter, two phase shifters (MZI arms) and a 2×2 MMI as the output power coupler. The 1×2 MMI is designed to have 50:50 power splitting ratio and connect equal-length (1-mm) phase shifters based on the zero-birefringence 3 μm × 3 μm strip waveguide. The aluminum pads (100 μm × 1000 μm) are placed on the side of the MZI arms for introducing driving voltage. By introducing forward bias voltage through the aluminium pad, carriers are injected into the optical waveguide and the refractive index changes. Therefore, the phase difference between two MZI arms can be adjusted with different driving voltage, and the input optical signal can be routed to desired output port in nanoseconds time (benefitting from the highly efficient plasma dispersion effect). The 12-channel 100 GHz spaced WDM input signal is demultiplexed by the Demux AWG to 12 individual 1×2 switching units, and each channel can be individually controlled and routed to one of two Mux AWGs. The two AWGs combine the selected wavelengths separately, and therefore the 1×2 WSS can provide seamless operation.

The 1×2 PIC-WSS were fabricated on the 3-μm ion-beam-trimmed silicon-on-insulator wafers with total thickness variation reduced below 100 nm. The i-line technology is used to transfer the pattern to the wafer, and the rib/strip waveguide structures are formed by double-step etching process. The n-type carrier injection region is completed by phosphorus ion implantation and the p-type carrier region is formed by boron ion implantation. The contact pads for voltage driving are deposited by sputtering aluminum films. The silicon nitride layer is deposited on input/output waveguide facets as anti-reflection coating to reduce the fiber-to-chip coupling loss. A 500-nm thick SiO_2 is deposited on the chip by plasma enhanced chemical vapor deposition (PECVD). Fig. 1 (c) illustrates the micrograph of the fabricated 1×2 WSS with compact size of 65 mm^2.

Experimental results

The experimental set-up for assessing the static and dynamic performance of the 1×2 WSS with WDM input signals and NRZ-OOK modulated signals is shown in Fig. 2. Firstly, the static characterization for recording the switching-on/-off spectra at two output ports in C-band was conducted. The switching performance was measured by injecting the light of a tunable laser source into the WSS input port via a polarization controller, and the output power of the two output ports were measured by optical spectrum analyzer (OSA). The DC forward-bias driving voltage was applied via the aluminium pads to each 1x2 switch by using a programmable voltage supplier.

Fig. 3 shows the switching on/off spectra of all channels switched to output port 1 and 2, respectively. Fig. 3 (a) show the switching ON at output 1 (solid curve) and OFF for output 2 (dashed curve). Around 0.9 V bias DC voltage is

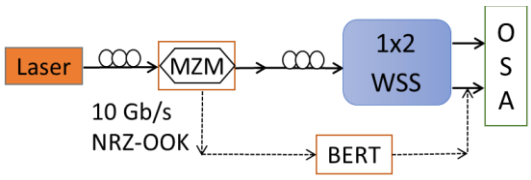

Fig. 2: The experimental set-up.

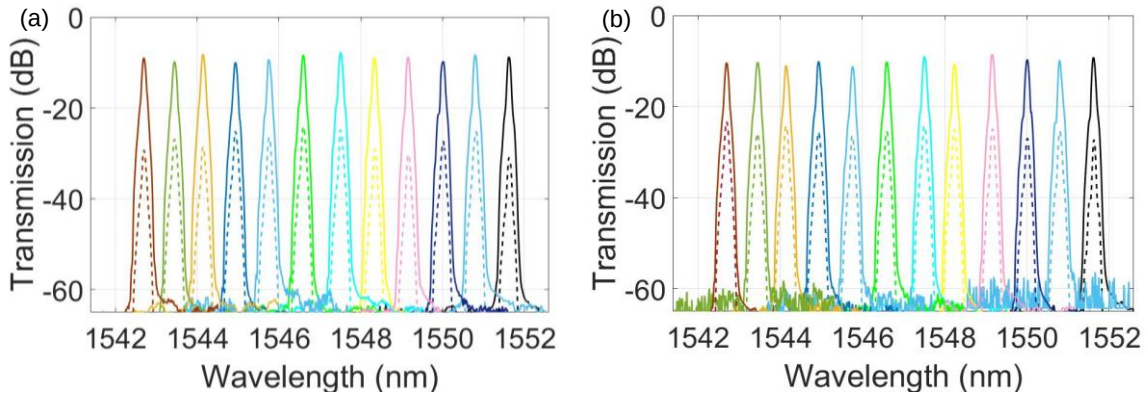

Fig. 3: (a) Output spectra of switching state A at 0.9 V voltage with solid curve for output 1 and dashed curve for output 2; (b) Output spectra of switching state B at 1.2 V voltage with solid curve for output 2 and dashed curve for output 1.

required for switching input signal to output port 1 (switching state A). For all 12 channels (1542.7 nm to 1551.7 nm), the insertion losses at output port 1 range from 7.8 dB to 10.1 dB, the extinction ratios between output 1 and 2 are from 16 dB to 23 dB, and the average channel spacing is ~ 101 GHz. Fig. 3 (b) shows the switching signal to output port 2 (switching state B, solid line) when around 1.25 V bias DC voltage is applied. The insertion losses at output port 2 are from 8.5 dB to 11.3 dB, the extinction ratios range from 14 dB to 19 dB. As the current 2x2 MMI coupler in the MZI switch provides unbalanced combining ratio for different wavelengths, higher extinction ratio can be achieved by optimizing the design of the 2x2 MMI. Most of the insertion loss (5 to 8 dB) is provided by the Demux and Mux pair insertion losses and slightly wavelength mismatching, while 1.5 dB loss from 1×2 MZI switching unit and remaining loss from waveguide crossings. The required RF switching voltage is around 0.35 V which results in ~ 70 mW power consumption for the switch. The switching time is measured by the oscilloscope and shown in Fig. 4 (a) with around 4.2 ns rising time and around 2.4 ns falling time.

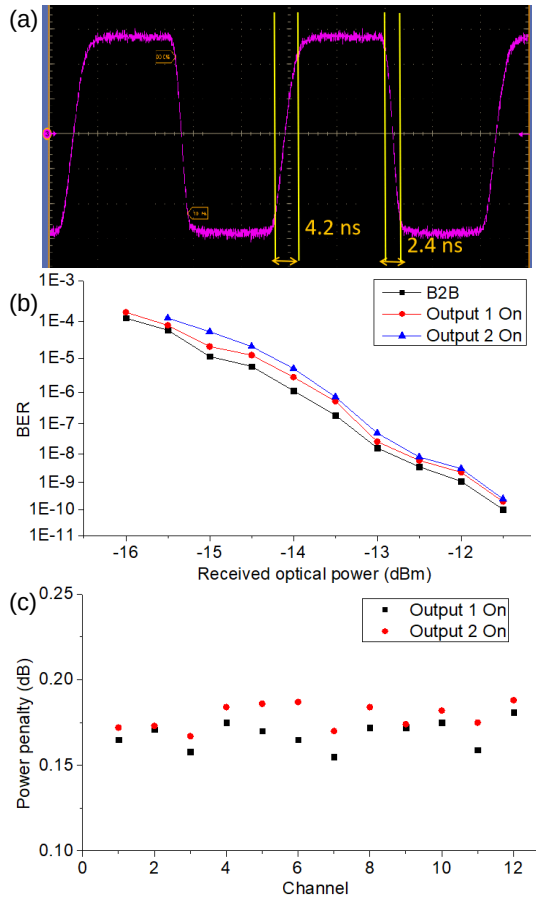

Fig. 4: (a) switching rising/falling time; (b) BER curves at 1547.72 nm; (c) error-free power penalty of all channels.

To quantify the 1x2 WSS performance with modulated data, the BER measurements were performed with 10 Gbit/s NRZ-OOK signal (PRBS 2^{31}-1). Results show error free operation with < 0.17 dB power penalty at 10^{-9} BER for 10 Gbit/s signal with 1547.72 nm switched to output 1 or 2 (see Fig. 4 (b)). Fig. 4 (c) demonstrates that for all 12 channels, the power penalty at 10^{-9} BER is < 0.2 dB at output 1 and 2.

Conclusions

We experimentally demonstrated a C-band nanosecond switching 1×2 PIC-WSS on 3-μm silicon platform. The experimental results show that the device has lowest insertion loss of 7.8 dB for switching to output 1 and 8.5 dB for switching to output 2, an average extinction ratio of ~ 19.5 dB, 4.2 ns switching rising time and 2.4 ns falling time, 0.35 V RF bias voltage and 70 mW power consumption. Error free operation at 10^{-9} BER has < 0.2 dB power penalty for 10 Gb/s data.

Acknowledgements

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