Accelerated Dark Current Degradation Study of Monolithically Integrated $In_{0.2}Ga_{0.8}As$/GaAs-on-Si Nano-Ridge Photodetectors

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Abstract *The reliability of $In_{0.2}Ga_{0.8}As$/GaAs nano-ridge photodetectors monolithically integrated on 300 mm Si substrates is first reported. Dark current increases and saturates at $2x10^{-5}$ A/cm^2 at 85 ℃ after stress, which is still sufficiently low. Carrier emission from pre-existing defects is identified as the dominant degradation mechanism.*

Introduction

Photodetectors (PDs) for silicon photonic (SiPho) applications require high speed, large photo-response, and low dark current. In addition, integration compatibility, production cost and reliability are decisive cornerstones for transferring the technology from research labs to the market.

Germanium possesses high light absorption in telecommunication wavelengths and Ge-on-Si (Ge/Si) waveguide PDs have exhibited high electro-optical bandwidth and high responsivity [1], [2]. However, ineffective Ge surface passivation and the presence of misfit defects at the Ge/Si interface, due to large lattice mismatch of 4 %, result in a relatively high dark current density (J_{dark}) in the order of 10^{-2} A/cm^2 [3]. On the other hand, III-V based semiconductors such as InGaAs, InAlGaAs, InGaAsP and GaAsSb are gain materials which can be employed for both light amplification and absorption; the various bandgaps in this family also enable selection of wavelengths ranging from visible light to mid-infrared. However, integration of III-V components on SiPho circuits usually relies on flip-chip bonding [4], which increases the cost and limits the scalability.

The monolithic integration of III-V materials on Si substrates could potentially achieve the lowest cost and the highest functionality, while similar to Ge/Si PDs, defects present at the surface and the III-V/Si interface need to be controlled [5]. Nano-ridge engineering (NRE) [6], which confines misfit defects in a narrow high-aspect trench and grows the active region outside the trench to ensure increased volume with high crystal quality, is one of the promising methods. Leveraging NRE and the InGaP passivation layers, $In_{0.2}Ga_{0.8}As$/GaAs nano-ridge waveguide PDs have demonstrated a record-low J_{dark} of $1.98x10^{-8}$ A/cm^2 and responsivity up to 0.65 A/W at room temperature [7]. However, the reliability of this device hasn't been investigated yet.

Despite many reports on realizing high-performance monolithically integrated PDs [8]–[10], limited reliability studies have been published. Standard tests on Ge/Si PDs indicate secured reliability [2], albeit wafer-level stress tests spotted defect generation and carrier filling of pre-existing states [11]. A bias-temperature stress of 120 h on InGaAs/Si p-i-n PDs showed a slight increase of dark current (I_{dark}), while the mechanism was not elucidated [12].

In this work, we present the first reliability assessment of monolithic $In_{0.2}Ga_{0.8}As$/GaAs-on-Si nano-ridge waveguide PDs, providing insights on the degradation mechanisms of I_{dark}.

Devices and Experiments

The $In_{0.2}Ga_{0.8}As$/GaAs nano-ridge p-i-n PDs were monolithically grown on Si substrate and fabricated in imec's 300 mm CMOS pilot line, using NRE and standard Cu metallization [7]. Devices with 2 diode lengths (100 μm and 1000 μm) and 2 contact pitches (0.6 μm and 4.8 μm) were compared in this study, as shown schematically in Fig. 1.

A package-level accelerated aging test was designed to investigate the overall trends of I_{dark} degradation. As shown in Fig. 2(a), a reverse voltage stress was applied at a bias of V_{stress} = -1 V, a temperature of T_{stress} = 125 ℃ and for a duration around 2000 h, with intermittent interruptions when cooling down to T_{sense} = 85 ℃ for I_{dark} readout.

Wafer-level degradation-mechanism-oriented tests aim to unveil defect kinetics, for which the test sequences are illustrated in Fig. 2(b). To begin with, all devices were aged using the same V_{stress} and T_{stress} as exerted in the package-level test, but for a shorter stress duration of 10 h without any interruption. Immediately after the electrical stress, one of the following two characterizations was performed: A. a static

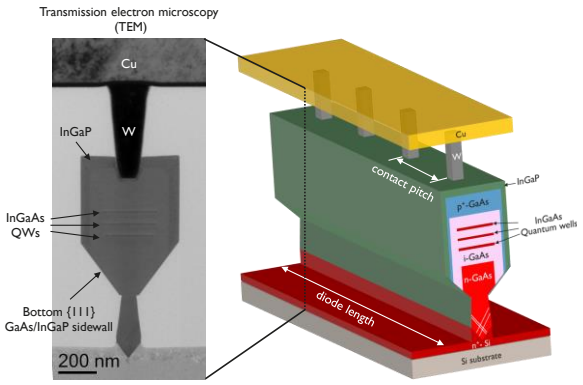

Fig. 1: A schematic of the InGaAs/GaAs p-i-n nano-ridge photodetectors monolithically grown on Si.

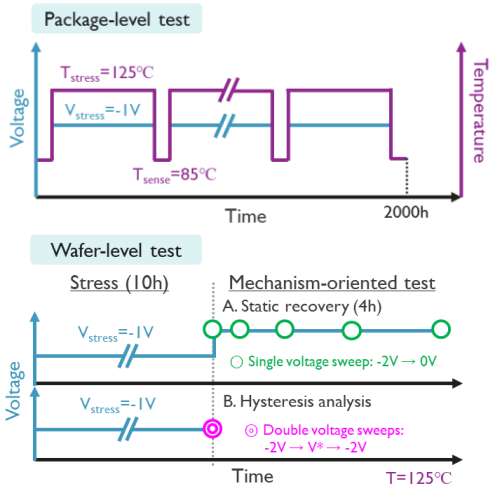

Fig. 2: (a) package-level bias-temperature stress; and (b) wafer-level degradation-mechanism-oriented tests, which either static recovery or hysteresis analysis was performed after 10h of stress.

recovery test that keeps devices under zero bias and measures I-V properties intermittently; or B. a hysteresis analysis which executes a double voltage sweep starting from -2 V to-and-from various assigned voltages (V*), with the relative hysteresis ($(I_1-I_2)/I_1$) extracted at V = -1 V.

The two-dimensional (2D) structure was simulated using TCAD Sentaurus Device in order to calculate and analyse the bias-dependent electric field (E-field) distribution throughout the nano-ridge. The Poisson equation was solved considering Fermi statistics as well as the density gradient quantization model.

Package-Level Bias-Temperature Stress

The relative change of I_{dark} (ΔI_{dark} / $I_{dark}(t = 0\ h)$) with respect to the stress time of 8 devices with 100 μm diode length and 0.6 μm contact pitch is shown in Fig. 3(a). I_{dark} increase generally follows a saturated power law, while some devices show a slight decrease after reaching a peak value. Fig. 4 depicts the maximum I_{dark} degradation of devices with different design parameters; longer devices display a higher level of I_{dark} increase, while no clear plug pitch dependence is

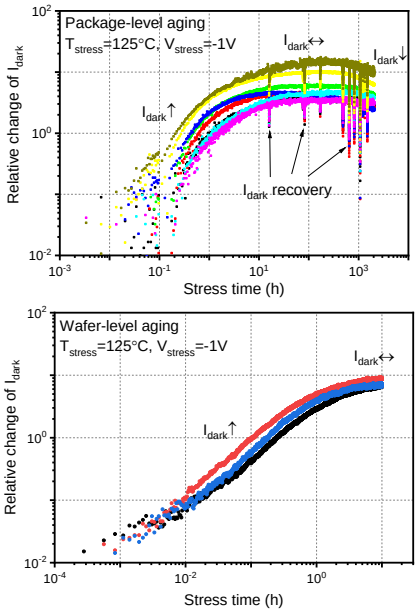

Fig. 3: Relative change of I_{dark} as a function of stress time: (a) Package-level stress reveals a 3-stage I_{dark} degradation. (b) Wafer-level stress only shows the saturated power-low increase of I_{dark} due to the shorter stress time.

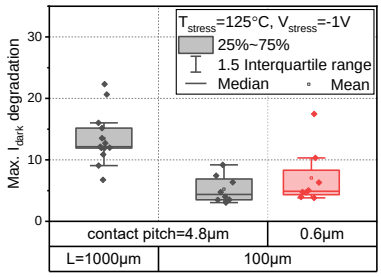

Fig. 4: Maximum I_{dark} degradation of different design parameters. Shorter devices degrade less, and no contact pitch dependence being found.

observed, offering the advantage of using sparse contact pitch to mitigate optical losses at metal plugs [7]. It is important to note that although there is some increase of I_{dark}, the monolithic $In_{0.2}Ga_{0.8}As$/GaAs-on-Si nano-ridge PD remains at a reasonably low I_{dark} after stress (max. J_{dark} ~ $2x10^{-5}$ A/cm^2 at T_{sense} = 85 °C). On top of the global tendency, a noticeable I_{dark} decrease was detected whenever the electrical stress was shortly interrupted (see Fig. 3(a)), which we postulate is linked to capture/emission of carriers at defect states.

Wafer-Level Stress-Recovery Test

For monolithic $In_{0.2}Ga_{0.8}As$/GaAs-on-Si nano-ridge devices, the main conduction mechanism at reverse bias is through trap-assisted tunnelling (TAT) [13]–[15]. Subsequently, the speculated model of I_{dark} increase during electrical stress is two-fold: a) the high E-field at reverse bias could promote emission of carriers from pre-existing defects, increasing the number of active defect states that can contribute to TAT; b) the generation of new defects. The former is often a

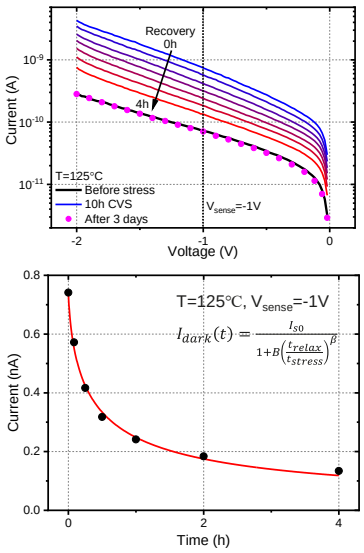

Fig. 5: Static recovery measurement: (a) I_{dark} is fully recoverable in full reverse voltage range. (b) a BTI-like model successfully describes the temporal I_{dark} recovery.

recoverable process since carriers can fill defect states again when electrical stress is removed, whereas the latter could permanently degrade the device properties. Therefore, inspecting I_{dark} recovery can help disentangling the contribution of these two mechanisms.

Wafer-level reverse voltage stress of 3 devices with diode length of 1000 μm and plug pitch of 4.8 μm are depicted in Fig. 3 (b), confirming a similar I_{dark} evolution as identified on package-level. Recovery of I-V characteristics after electrical stress is portrayed in Fig. 5. Remarkably, I_{dark} of the same post-stressed device, probed again 3 days after the test, demonstrates a near-complete recovery. The observation justifies carrier emission from pre-existing defect states as the dominant degradation mechanism that increases I_{dark}. It is noteworthy that this model also explains the saturation of I_{dark}, as the number of pre-existing defect states is finite, I_{dark} will reach a maximum when all trapped carriers are expelled. Furthermore, I_{dark} as a function of recovery time is outlined at V = -1 V and plotted in Fig. 5(b). A semi-empirical defect kinetics model, analogous to that of bias-temperature instability (BTI) [16], successfully describes the measured data, providing a rough estimation of capture time constant τ_c = 1/B ~ 360 s.

Hysteresis Analysis and 2D E-field Simulation

Hysteresis in a current-voltage characteristic is a signature of defects which change their charge states during repeated measurements. As shown in Fig. 6, double voltage sweeps in reverse bias region (V* < 0 V) yield negligible hysteresis, on the contrary hysteresis increases when extending the sweep to higher forward bias (V* >

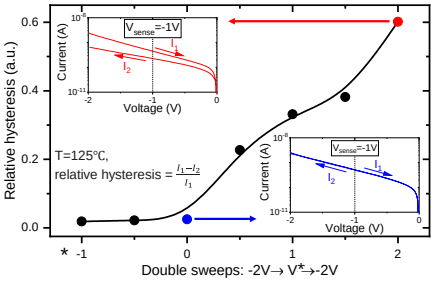

Fig. 6: Hysteresis increases when sweeping to forward bias region because of the accelerated recovery of I_{dark}.

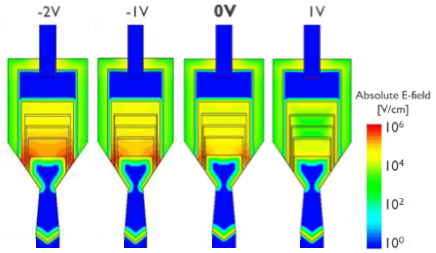

Fig. 7: 2D TCAD simulation: high E-field at the bottom {111} sidewalls can be alleviated by sweeping to forward bias.

0 V). The more pronounced I_{dark} recovery in forward region can be attributed to the joint effect of reduced E-field and proliferation of free carriers, which accelerates the carrier capture process at defect states.

The increase of I_{dark} during stress is suspected to arise from bottom {111} GaAs/InGaP sidewalls because of the relatively thin InGaP surface passivation (~ 5 nm), which might lead to poorer carrier confinement and faster recombination. Besides, previous study has proven that the surface-state density is positively correlated with I_{dark} [15]. Simulated absolute E-field contours shown in Fig. 7 reinforce this hypothesis. High E-field at the bottom {111} GaAs/InGaP sidewalls is alleviated when sweeping from reverse to forward bias, thus reduces carrier capture time constant and increases hysteresis.

Conclusions

Accelerated aging of monolithic GaAs/Si p-i-n nano-ridge photodetectors is presented in this work, including both the package-level standard test and wafer-level tests dedicated to understanding degradation mechanisms. J_{dark} increases and saturates at around $2x10^{-5}$ A/cm^2 at T = 85 °C, which is still sufficiently low after the bias-temperature stress of 2000 h. Detailed reliability studies indicate that carrier emission at pre-existing defect states is the dominant mechanism, which possibly originates from surface states at {111} GaAs/InGaP sidewalls.

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