A Lateral Interleaved P-well/N-well Photodetector with Enhanced Transit-Time Bandwidth in 28-nm CMOS

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Abstract *A transit-time-enhanced silicon photodetector is proposed and fabricated in standard CMOS without process modification. By adopting the lateral interleaved junction, this PD features a 0.13-A/W responsivity and a doubled 10.43-GHz transient-time bandwidth. Moreover, a clear 10-Gb/s 850-nm optical eye diagram is observed.*

Introduction

Research on electronic-photonic integrated circuits (EPIC) in a process with economic, performance and power potential for high volume manufacturing such as CMOS is highly desirable both for 850-nm multi-mode fiber (MMF) and 1310/1550-nm single mode fiber (SMF) applications [1]. In fact, the manufacture of EPIC for SMF systems requires a deep reconstruction of CMOS process and only a few foundries have the capability and finance to do. On the other hand, since visible and 850-nm light can be detected by silicon, cost-effective EPIC receivers (Rxs) can be easily realized in CMOS or BiCMOS process, taking a full advantage of powerful silicon technology such as low-cost fabrication and high-volume manufacturability. This makes EPIC Rxs potentially applicable to hyperscale data centers and high-performance computer networks [2]. In monolithic CMOS Rxs, developments of high-speed CMOS photodetectors (PDs) are the most critical issue due to their bandwidth limitations [3]. The bandwidth of PDs is mainly limited by the photo-generated carrier transit-time and RC parameters of PN junction. By leveraging pre- and post-equalization techniques such as the feed-forward equalizer (FFE), continuous-time linear equalizer (CTLE), and decision-feedback equalizer (DFE), the RC bandwidth of PD can be extremely extended [4-6]. However, the improvement of transit-time bandwidth of CMOS PDs is rarely reported.

In this work, we propose and demonstrate a silicon P-well/deep N-well (PW/DNW) PD with lateral interleaved PW/NW junction. The proposed PD has been implemented in 28-nm CMOS technology. For comparison, one traditional PW/DNW PD have been implemented in the same tapeout run. The transit-time bandwidths of two types of PDs have been extracted by the equivalent circuit model. With the lateral interleaved P/N-well junction, the transit-time bandwidth of PW/DNW PDs has been improved significantly.

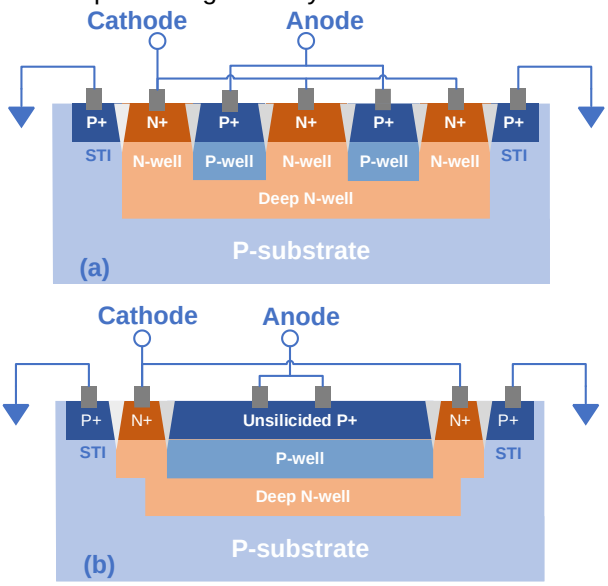

Fig. 1 Cross-section views of the PW/DNW PDs (a) PD1 with and (b) PD2 without lateral interleaved PW/NW junction.

Device Design and Work Principle

A CMOS PD with a deep N-well has been recognized as an effective method to increase the bandwidth [7]. In our previous work, monolithic CMOS Rxs with the PW/DNW PD has demonstrated an 18-Gb/s record-high data rate in 65-nm CMOS [5, 8]. Figure 1(a) and 1(b) show the cross-section views of the PW/DNW PDs with and without the lateral interleaved PW/NW junction, respectively. For high-speed operation, the electric field of the PN junction should match as closely as possible to the optical field in the absorption region [9]. In the PW/DNW PD, the depletion region only spans in the interface of P-well and Deep N-well region. As the PD is top-illuminated, large part of photo-generated carries in the P-well region can only diffuse to the depletion region, leading to the low transit-time bandwidth. The PW/DNW PD with lateral interleaved PW/NW can effectively enlarge the depletion region at the photocarrier-generated region. Additionally, the lateral interleaved

PW/NW may increase the value of junction capacitance and series resistor. Therefore, the number of interleaved PW/NW junctions should be employed properly. Here, we design 5-tap interleaved PW/NW junctions to enhance transit-time bandwidth at low cost of RC bandwidth.

Measurement Results

Figure 2 shows the chip microphotograph of two PDs fabricated in 28-nm CMOS. For simplicity, we set that PD1 is the PW/DNW PD with lateral interleaved PW/NW junction, and PD2 is without that junction. Both PDs have a size of 10*10 μm^2. The measured DC characteristics results are shown in Fig. 3. Under –5V bias voltage, the dark currents of PD1 and PD2 are 6.84 and 9.52 nA, respectively. The photocurrent is measured under an illuminated power of 316 μW. Therefore, the responsivities at 850-nm wavelength of PD1 and PD2 are 0.13 and 0.125 A/W, respectively.

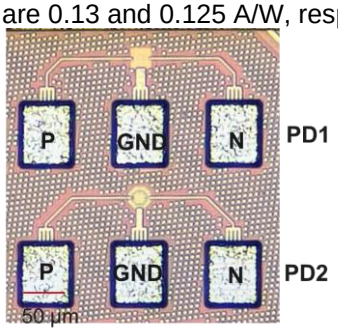

Fig. 2 Chip microphotograph of PDs with (PD1) and without (PD2) lateral interleaved PW/NW junction.

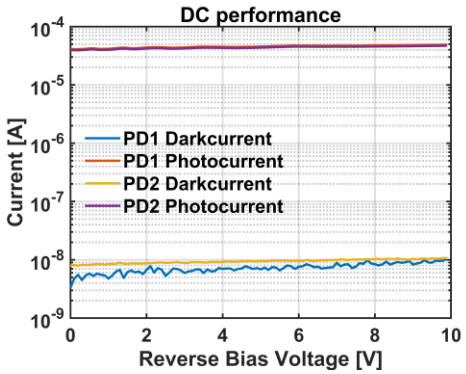

Fig. 3 DC performance of PD1 and PD2

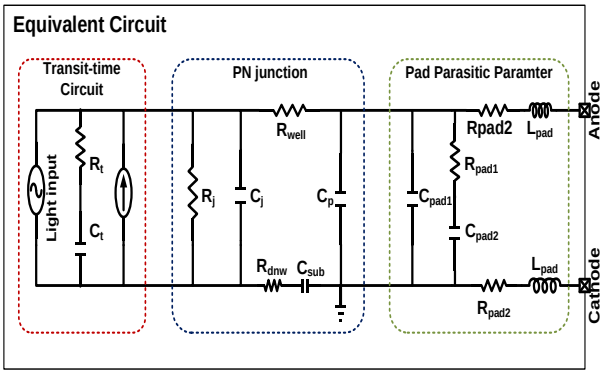

Fig. 4 Equivalent circuit of CMOS PDs.

To accurately extract the transit-time bandwidth, the equivalent circuit model is presented in Fig.4 [10]. The equivalent circuit contains three parts, which are the transit-time circuit, the PN junction, and parasitic parameters. The S-parameter of PD is measured by the light component analyser (LCA). The parasitic parameters of pads and electrodes are extracted from additional open and short testing structures. The RC of PN junction can be extracted from the S-parameter results. Figure 5 shows the measured and simulated S-parameter results of PD1 and PD2 under -5V reverse bias voltage, respectively. These S_{11} fitting results agree well with the measured results. Both simulated and measured S_{21} results show that the optic-electrical (OE) 3-dB bandwidth of PD1 and PD2 are 4.53 and 3.27 Hz, respectively. The details of equivalent circuits are listed in Table 1. As shown in Tab. 1, the junction capacitance of PD1 is larger than PD2, due to the interleaved junction. However, the transit-time bandwidths of PD1 and PD2 are 10.43 and 5.95 GHz, respectively, which are calculated by the equation: $1/(2\pi R_t C_t)$. These results prove that an over 140% improvement in the transit-time bandwidth, with an acceptable decrease in the RC bandwidth. Therefore, the OE bandwidth of PD1 is larger than the bandwidth of PD2.

Tab. 1: Equivalent circuit parameters of CMOS PDs

Component	PD1	PD2	Description
C_t [fF]	305	535	Equivalent transit-time capacitor
R_t [Ω]	50	50	Equivalent transit-time resistor
R_j [Ω]	1.48M	1.78M	Junction resistor
C_j [fF]	54	32	Junction capacitor
R_{well} [Ω]	140	195	Series resistor from PW/NW
R_{dnw} [Ω]	102	148	Series resistor from deep N-well
C_{sub} [fF]	10.28	12.77	Substrate capacitance

To further evaluate the performance, the transient eye diagram measurement is implemented. Figure 6 shows the measurement setup for PDs' optical eyes. The electrical signal is generated from the bit error ratio tester (BERT, Keysight, M8040A), then modulated into the optical domain by the 850-nm reference transmitter (Tx, Keysight, 81491A). The optical

signal is in non-return-zero (NRZ) format with pseudo random bit sequence (PRBS) of 2^{15}-1. The modulated signal is coupled into the device under test (DUT) by the multimode fiber.

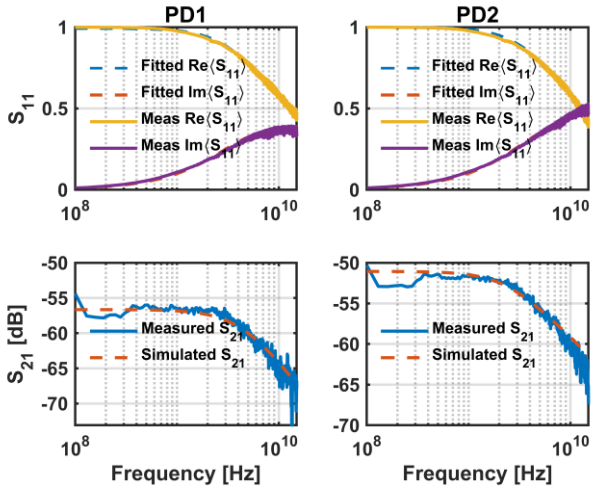

Fig. 5 Measured and simulated S-parameter results of PD1 and PD2.

Before being sampled by the oscilloscope (Keysight, N1092), the electrical signal from the DUT is amplified by a commercial amplifier (iXblue, DR-AN-10-MO). Figure 7 shows PD1's optical eye diagrams with and without one 5-tap FFE. A clear eye diagram with a Q-factor of 3.82 can be observed from the oscilloscope. Suffering low bandwidth of the PD2, no clear eye diagram can be observed from the PD2.

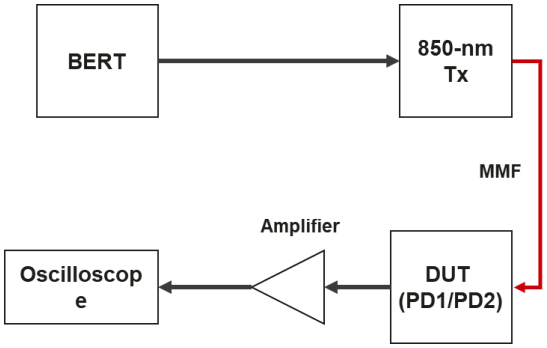

Fig. 6 Measurement setup for PDs' optical eyes.

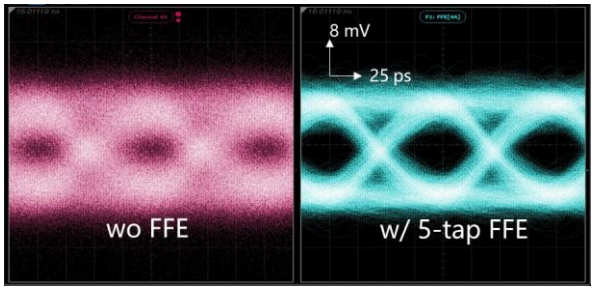

Fig. 7 Measured 10-Gb/s eye diagrams of PD1 without and with 5-tap FFE.

Tab. 2: Performance comparison to recently reported CMOS PDs

	[6]	[8]	This work	
CMOS Tech. [nm]	130	65	28	
PD Structure	P+/N-well	P-well/DN-well	Interleaved PW/NW (PD1)	P-well/DN-well (PD2)
Gain/responsivity [A/W]	1/0.05	1/0.05	1/0.13	1/0.125
Bandwidth [GHz]	0.348	0.051	4.53	3.27
Transit-time bandwidth [GHz]	NA	NA	10.43	5.95
Area [μm^2]	70*70	50*50	10*10	10*10
Bias Voltage [V]	1.5	1	5	5

Conclusions

One transit-time-enhanced CMOS PD is proposed and demonstrated in standard 28-nm CMOS without process modification. Table 2 compares this work with state-of-the-art works. The measured OE bandwidth of the proposed PD is 4.53 GHz. More importantly, the extracted transit-time bandwidth is larger than 10 GHz. The post layout simulation suggests that the monolithic CMOS Rxs with this PD can achieve over 25-Gbaud signal receiving by leveraging pre- and post- equalization techniques.

Acknowledgement

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