Real-time FPGA Prototyping of High Sensitivity 15Gbps 4PPM-QPSK Receiver

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Abstract *We demonstrated a real-time high sensitivity 15Gbps 4PPM-QPSK receiver based on a single FPGA chip. An efficient PPM symbol synchronization scheme has been realized. In the real-time experiment, the receiver achieved a sensitivity of -48dBm at BER of 1E-3. ©2023 The Author(s)*

Introduction

For most optical transmission systems, especially the signal power limited ones like the free space optics system, the receiver sensitivity is one of the most important characteristics. The sensitivity is always given in the received optical power (ROP) or the photons per bit (PPB). To pursue a higher receiver sensitivity, plentiful works have been reported as shown in Tab. 1. Among these modulation formats, the pulse position modulation (PPM) technique has been proposed and has been widely used in the satellite communication systems [1]. The PPM signals' energy is only concentrated in some of the time slots during one PPM symbol period, while the energy is nearly zero in the rest of slots. Thus, compared to the commonly used modulation formats in the fibre optical communication system like OOK, BPSK and QPSK, PPM is much more power-efficient. Besides, PPM can also be combined with the coherent modulation formats, e.g., PPM-BPSK and PPM-QPSK, to achieve even higher sensitivity and bit rate [2].

At present, several researches about real-time PPM system have been reported. Among these works, the highest reported bit rate before this work is 1.25Gbps [3]. However, as the clock frequency of real-time digital signal processing (DSP) chips, e.g., field programmable gate array (FPGA) and application specific integrated circuit (ASIC), is at the order of several hundred megahertz, when it comes to a high-bit-rate PPM receiver, the DSP must be organized in a parallel structure to meet the demand of real-time throughput. Therefore, the real-time DSP scheme for high-bit-rate PPM system is still waiting for investigation.

In this work, we demonstrated a real-time 4PPM-QPSK receiver with the world's highest bit rate of 15Gbps. The receiver DSP, including the clock recovery, PPM symbol synchronization and the carrier recovery, is realized in a single FPGA

Tab. 1: Reported high sensitivity receivers

Format	Bit rate	ROP	PPB
BPSK	10Gbps	-47dBm@1E-3 (offline) [4]	11.9dB
	40Gbps	-36dBm@1E-3 (real-time) [5]	16.9dB
DPSK	2.5Gbps	-58.2dBm@3E-3 (offline) [6]	6.74dB
QPSK	10.52Gbps	-49.8dBm@1E-3 (offline) [1]	8.90dB
	106Gbps	-34dBm@1E-3 (real-time) [7]	14.7dB
16-PPM	1.25Gbps	-46.2dBm@3.3E-5 (real-time) [3]	21.8dB
16PPM-QPSK	2.5Gbps	-59.5dBm@1E-3 (offline) [2]	5.44dB
4PPM-QPSK	7.5Gbps	-55.9dBm@1.5E-2 (offline) [2]	4.27dB
	15Gbps	-48dBm@1E-3 (real-time, this work)	9.16dB

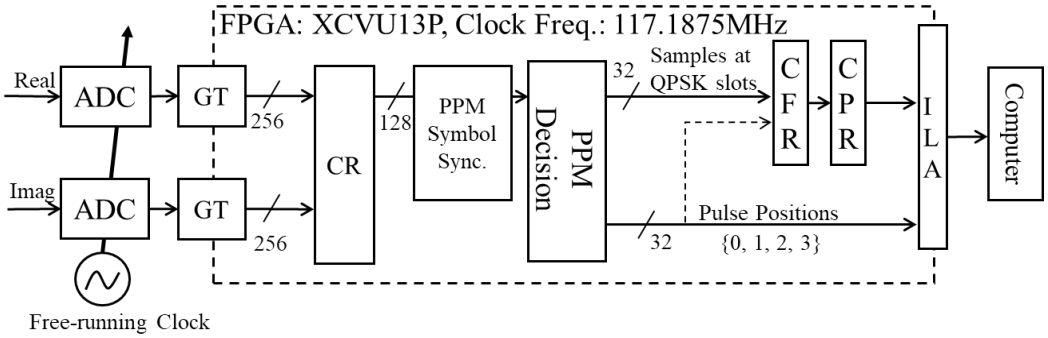

Fig. 1: The scheme of the real-time 4PPM-QPSK receiver DSP. ADC: analog-to-digital convertor; GT: gigabit transceiver; CR: clock recovery; CFR: carrier frequency recovery; CPR: carrier phase recovery; ILA: integrated logic analyzer.

chip. In the real-time experiment, the receiver achieved a sensitivity of -48dBm at bit error rate (BER) of 1E-3, which has a gap of 4.6dB compared to the theoretical limit [2].

Real-time 4PPM-QPSK Receiver DSP

The FPGA-based receiver DSP of 4PPM-QPSK receiver is illustrated in Fig. 1. Among these modules, the clock recovery and carrier phase recovery are simply modified from the real-time 16QAM receiver introduced in our previous work [8]. The major different DSP modules between the 4PPM-QPSK receiver and the 16QAM/QPSK receiver are the symbol synchronization, the PPM decision and the carrier frequency recovery.

The clock recovery is realized by Gardner algorithm with a 7-tap sinc interpolator. With the help of clock recovery, the sampled signals with an oversampling rate of 2 samples per slot are converted to 1-sample-per-slot signals without sampling phase errors [8].

The symbol synchronization is essential because the information carried by the pulse positions can only be extracted when the edge of PPM symbols is correctly distinguished [3]. The core idea is that, during one PPM symbol period, since there is only one time slot that carries power, the edge of PPM symbols must locate at the middle of two consecutive power-carrying slots. Fig. 2 shows an example, where the second edge of PPM symbols can be located through the above-mentioned method. In the real-time implementation, the DSP processes 128 time slots, i.e., 32 4PPM symbols, in every clock cycle. Once the position of one symbol

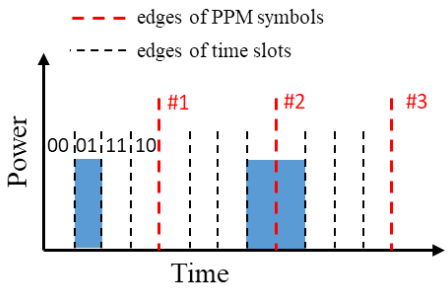

Fig. 2: An example of 4PPM time slots and 4PPM symbols. The dashed lines indicate the edges of symbols and slots.

edge is determined, the positions of the other symbols are also determined.

After the PPM symbol synchronization, the PPM decision can be correctly performed. Symbols can be separated from each other according to the positions of edges. In every PPM symbol, the QPSK symbol is extracted from the time slot with the highest power, whose position is also extracted. The QPSK sequence and the pulse positions are fed into the following modules.

As for the carrier frequency recovery, unlike the traditional coherent QAM receiver, the extracted QPSK symbols from PPM-QPSK signals are not continuous in time, and the frequency offset between two adjacent QPSK signals is not uniformly accumulated but determined by the pulse positions. The (n-1)-th QPSK symbol can be expressed as

$$S_{n-1} = \exp[\, j(\theta_{QPSK,n-1} + \theta_{bias,n-1})] \qquad (1)$$

The symbol $\theta_{QPSK,n-1}$ denotes the original phase of the (n-1)-th QPSK symbol, which can be π/4, 3π/4, 5π/4 or 7π/4. The symbol $\theta_{bias,n-1}$ denotes the accumulated phase bias caused by frequency offset, phase noise and other phase-related effects. Then, the n-th received QPSK symbol S_n can be expressed as

$$S_n = \exp\{\, j[\theta_{QPSK,n} + \theta_{bias,n-1} + 2\pi\Delta f\,(4 + P_n - P_{n-1})T_s\,]\} \qquad (2)$$

The symbol Δf is the carrier frequency offset. P_n denotes the pulse position of the n-th 4PPM symbol, which can be 0, 1, 2 or 3. The symbol T_s is the period of time slots. Therefore, the frequency offset can be obtained by dividing the phase difference between two adjacent QPSK symbols by the number of time slots between them.

Real-time back-to-back Experiment

The receiver DSP described in the previous section was realized in an FPGA chip (model: XCVU13P). The resource utilization is listed in Tab. 2. The used resource includes the ADC-FPGA interface, the DSP modules and the modules for storage. Except the BRAM, which was mainly used for storing the signals for further analysis, the real-time DSP only consumes less than 1/4 of the total resources of the FPGA.

Tab. 2: Resource utilization of the FPGA chip

Resource	Amount/Total	Utilization
LUT	372.3K/1728K	22%
Reg.	419.3K/3456K	12%
CARRY8	30.7K/216K	14%
BRAM	1083/2688	40%
DSP48	631/12.3K	5%

All experimental results in this paper were obtained based on the back-to-back experiment shown in Fig. 3. In this paper, we treated the ROP when the pre-forward-error-correction (FEC) BER of the received signals reaches 1E-3 as the sensitivity of the system. At the transmitter, a commercial four-port laser source with a linewidth of ~100KHz was used. One laser source was used as the transmitter carrier injected to an IQ modulator and another laser source was used as the local oscillator (LO). Two 7.5Gbps pseudo-random bit sequences (PRBS) were used to form

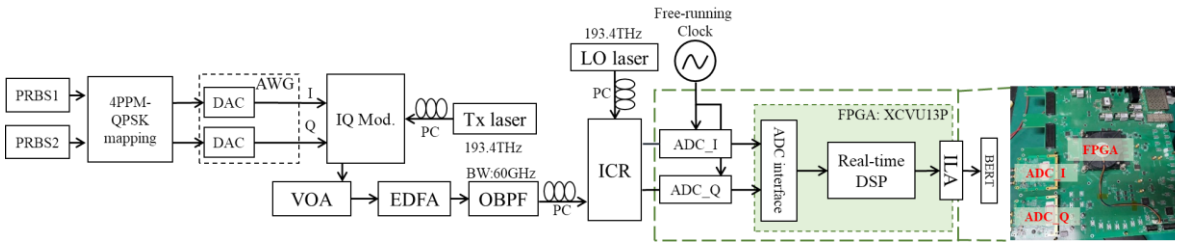

Fig. 3: Schematic of back-to-back experiment setup. PC: polarization controller. AWG: Arbitrary waveform generator. VOA: variable optical attenuator. EDFA: Erbium Doped Fiber Amplifier. OBPF: optical bandpass filter. ICR: integrated coherent receiver. LO: local oscillator. BERT: bit error rate test. ILA: integrated logic analyzer.

a 4PPM sequence and a QPSK sequence, respectively. These two sequences were then combined to generate the 15Gbps 4PPM-QPSK signals with a time slot rate of 15Gslots per second. After that, the in-phase (I) and quadrate (Q) components of the signals were transmitted to an arbitrary waveform generator (AWG) with two 60GSa/s digital-to-analog converters (DACs). The DAC outputs were amplified to a peak-to-peak voltage swing of 7V and drove the IQ modulator (with 3dB bandwidth of 22GHz). The IQ modulator outputted a 15Gbps optical 4PPM-QPSK.

To measure the receiver sensitivity, the generated signal output from IQ modulator was attenuated by a variable optical attenuator (VOA). The signals then entered an EDFA and were boosted to 8dBm. Meanwhile, an OBPF was used to filter out the out-band noise before being received by the receiver.

At the receiver, the optical signals and LO carrier were input into an ICR (with a 3dB bandwidth of 22GHz and integrated trans impedance amplifier) and were converted into electrical signals. Finally, the electrical signals were sampled by two 6-bit analog-to-digital convertors (ADC, with an effective noise of bits of 4.3 at 14GHz) driven by a free-running clock. The clock signals were generated by an external RF generator. To achieve an oversampling rate of 2 samples per slot, the frequency of the clock signal is set to 15 GHz, enabling ADCs to sample the received signal at 30GSa/s. The sampled signals were processed by the real-time DSP in the FPGA. The results of real-time DSP were stored and transmitted to the computer for further analysis.

To measure the sensitivity curve of the receiver, we collected hundreds of groups of recovered constellations within 5 minutes running of FPGA for BER under each ROP. Each constellation was composed of 131072 4PPM-QPSK symbols. The time slots carrying no energy scattered around (0,0) on the complex plane (see the constellations captured after clock recovery in Fig.4). The slots carrying energy located in the outer ring of the constellations. The final BER is obtained by comparing the captured signals to the transmitted PRBS sequences without any FEC. Fig. 4 shows that the real-time

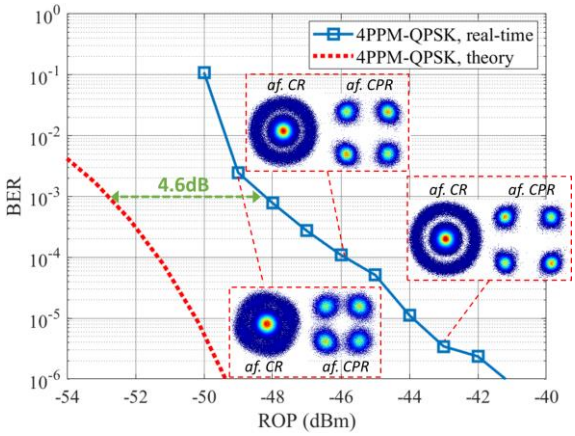

Fig. 4: The ROP versus BER measured in the real-time experiment and the constellations after clock recovery and carrier phase recovery captured from the real-time DSP.

DSP worked on a single FPGA chip successfully when the ROP was above -49dBm. When the ROP was lower than -49dBm, the BER jumped to above 0.1 and the DSP failed to demodulate the signals due to the cycle slip [9]. From these results, it's clear that the real-time 4PPM-QPSK receiver achieved a receiver sensitivity of -48dBm at BER of 1E-3. We also calculate the theoretical sensitivity of 4PPM-QPSK based on [2]. Compared to the theoretical limit, a sensitivity gap of 4.6dB at BER of 1E-3 can be observed.

Conclusion

In this paper, for the first time, we realized a real-time 4PPM-QPSK receiver with the highest bit rate of 15Gbps. A practical real-time DSP scheme was introduced, which has an advantage of low complexity. The high sensitivity of the proposed receiver (-48dBm at pre-BER of 1E-3) was proved through the real-time back-to-back experiment.

Acknowledgements

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