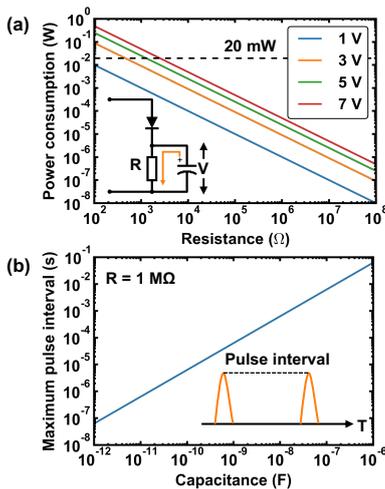




capacitor.

To evaluate the power consumption of the charge dissipation through the RC circuit, we consider the pulse control case. This means the frequency of the input pulse is much faster than the charge dissipation speed in the RC component, and the voltage of the capacitor is almost constant. The leakage in the MOS phase shifter is small and the power consumption is also ignorable ( $< 1$  nW [9]). Thus, the power consumption of the parallel resistor is the dominant part. Figure 2(a) shows the power consumption with different resistance values under different voltages on the MOS capacitor. Although the higher resistance leads to lower power consumption, the higher resistance results in the slower charge dissipation time. To achieve the balance between the power consumption and operation speed, we chose 1 M $\Omega$  resistor in the later experiments. It is expected to achieve 500 times smaller power consumption compared with TO phase shifters even with 7V bias.

The resistance value also affects the RC constant for the dissipation state, which is related to refreshing speed in pulsed control. Thus, there is a trade-off between power consumption and refreshing speed. Fig. 2(b) shows the maximum pulse interval as a function of the capacitance of the MOS capacitor. With 1 M $\Omega$  resistor and the III-V/Si MOS phase shifter ( $< 1$  pF), the pulse interval can be below 0.1  $\mu$ s, which is much smaller than TO phase shifter (2  $\mu$ s [4]), indicating a faster refreshing speed.

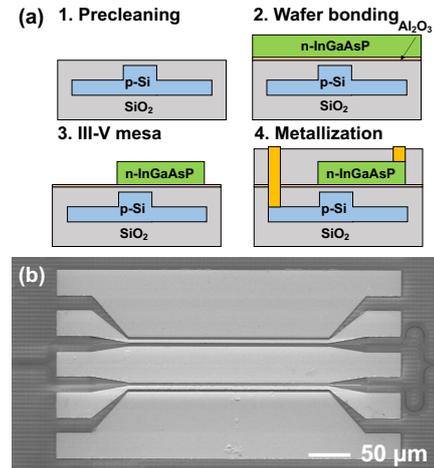


**Fig. 2:** (a) Power consumption of parallel resistors under different biases. (b) Maximum pulse interval for different MOS capacitance values with 1 M $\Omega$  resistor.

### Device fabrication

To demonstrate the crossbar wiring scheme with the III-V/Si MOS phase shifters, an asymmetric MZI modulator was fabricated. Figure 3(a) shows

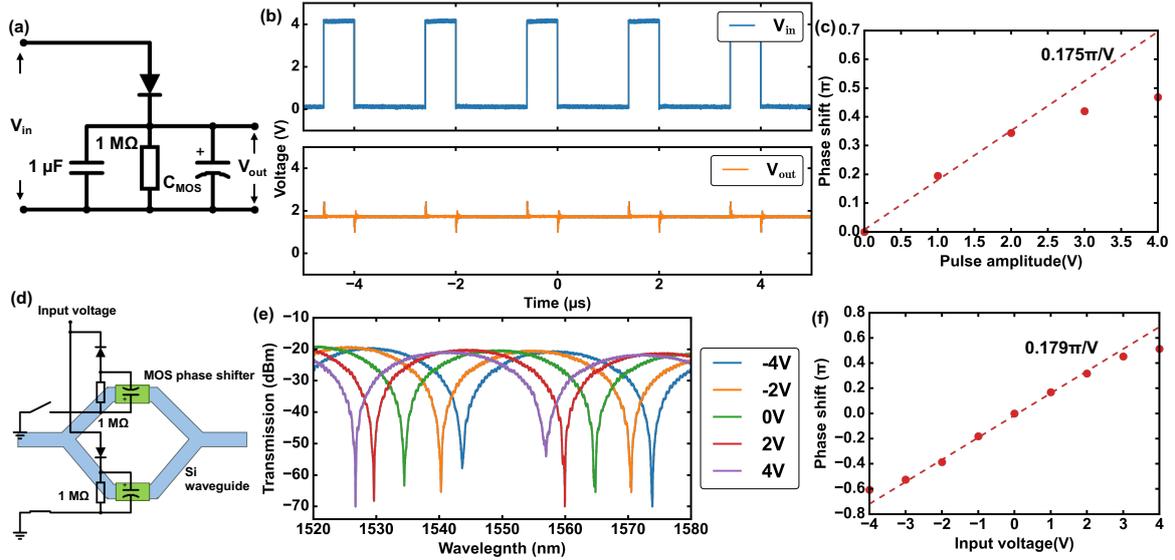
the fabrication procedure. Firstly, we started from a 220-nm Si-on-insulator (SOI) wafer. After ion implantation, the Si waveguide was defined by lithography and reactive-ion etching (RIE). A SiO<sub>2</sub> layer was deposited on the surface by tetraethoxysilane (TEOS) based plasma-enhanced chemical vapor deposition (PECVD). Followed by the chemical mechanical polishing (CMP), a 200-nm-thick n-In<sub>0.97</sub>Ga<sub>0.21</sub>As<sub>0.46</sub>P<sub>0.54</sub> layer grown on an InP substrate was bonded upon the Si waveguide with a 20-nm-thick Al<sub>2</sub>O<sub>3</sub> bonding interface deposited by atomic layer deposition (ALD). After bonding, the InP substrate and buffer layers were removed by chemical etching. Then, the mesa for the InGaAsP layer was defined by lithography and RIE. Finally, a SiO<sub>2</sub> cladding was deposited by PECVD and metal pad (Ni/Au) was formed by lift-off process. Figure 3(b) shows the plan-view scanning electron microscopy (SEM) image of the fabricated asymmetric MZI modulator.



**Fig. 3:** (a) Process flow for fabricating III-V/Si hybrid MOS optical phase shifters. (b) Plan-view SEM image of the fabricated asymmetric MZI modulator.

### Experimental results

Figure 4(a) shows the circuit for demonstration of the pulse-amplitude control with the III-V/Si MOS optical phase shifter. We added a 1- $\mu$ F parallel capacitor to tune the RC constant due to the limited speed of the waveform generator. A square-wave voltage pulse with a frequency of 500 kHz and a duty ratio of 30% was input, and Fig. 4(b) shows the waveform of the input pulses with an amplitude of 4 V ( $V_{in}$ ) and the voltage at the optical phase shifter ( $V_{out}$ ). Clearly, we obtained the constant voltage output for the MOS phase shifter with the pulse input. Note that the ringing at the pulse edges was due to a parasitic reactance in the circuit and can be removed by the circuit optimization. With the pulse input, the phase shift was measured as shown in Fig. 4(c).



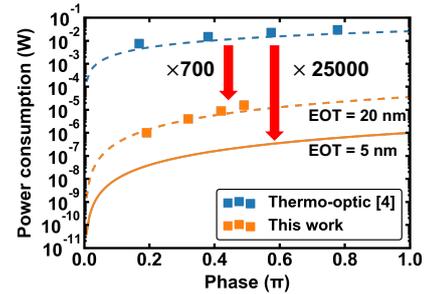
**Fig. 4:** (a) Equivalent circuit for the demonstration of pulse amplitude control with III-V/Si MOS optical phase shifter. The  $C_{\text{MOS}}$  represents one phase shifter on one arm of the asymmetric MZI modulator. (b) Input voltage waveform and measured output voltage waveform of the MOS optical phase shifter. (c) Measured phase shift with different pulse amplitudes. (d) Schematic of crossbar wiring with two phase shifters in asymmetric MZI modulator. (e) Measured spectra with different input voltages. (f) Measured phase shift with different input voltages.

The optical phase shift increased linearly with the pulse amplitude up to 2 V, with a modulation efficiency of  $0.175\pi/\text{V}$ . The measured phase shift reached  $0.48\pi$  with 4V amplitude, which can be further improved by using thinner gate oxide for the MOS phase shifter. Note that the saturation in the phase shift with amplitude over 2 V is due to leakage in the MOS capacitor.

Next, the selection functionality of the crossbar wiring scheme is verified using two MOS phase shifters in the asymmetric MZI modulator as shown in Fig. 4(d). Since the electrode for the Si slab was shared between two phase shifters, we flipped the direction of the diode for the phase shifter at the upper arm and used polarized voltage input to achieve the selection function. When the input voltage is positive, the lower row is connected while upper row is isolated, and vice versa. Figure 4(e) shows the measured spectra with biases from  $-4\ \text{V}$  to  $+4\ \text{V}$ . The measured phase shift is shown in Fig. 4(f). A linear phase shift is achieved regardless of the voltage polarity and successfully verified the selection function of the crossbar wiring scheme.

Finally, Figure 5 shows the benchmark of power consumption versus phase shift between the III-V/Si MOS phase shifter and TO phase shifter in crossbar wiring schemes. The solid and dotted lines show the numerical analyses, and square dots are experimental results. The experimental result shows the III-V/Si hybrid MOS phase shifter exhibits 700 times lower power consumption than the TO phase shifter reported in [4]. By further reducing the equivalent oxide thickness (EOT) of the MOS capacitor, a

much lower power consumption of 25000 times smaller can be achieved with much lower driving voltage.



**Fig. 5:** Benchmark of power consumption between the hybrid MOS optical phase shifter and TO phase shifter in crossbar wiring scheme.

## Conclusions

We proposed a crossbar wiring scheme with diode selectors for voltage-driven III-V/Si hybrid MOS optical phase shifters. We demonstrate the pulse-amplitude control of the MOS optical phase shifter with a diode selector and verified the selection function. Our experimental result shows 700 times lower power consumption than the TO phase shifters for crossbar wiring. This crossbar wiring configuration is expected to be a practical solution for reducing the number of the electrical contacts for phase shifters in large-scale programmable PICs.

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## References

- [1] Y. Shen, N. C. Harris, S. Skirlo, M. Prabhu, M. Hochberg, X. Sun, S. Zhao, H. Larochelle, D. Englund, and M. Soljačić, "Deep learning with coherent nanophotonic circuits," *Nature Photonics*, vol. 11, no. 7, pp. 441–446, 2017, DOI: [10.1038/nphoton.2017.93](https://doi.org/10.1038/nphoton.2017.93).
- [2] J. Carolan, C. Harrold, C. Sparrow, E. Martín-López, N. J. Russell, J. W. Silverstone, P. J. Shadbolt, N. Matsuda, M. Oguma, M. Itoh, G. D. Marshall, M. G. Thompson, J. C. F. Matthews, T. Hashimoto, J. L. O'Brien, and A. Laing, "Universal linear optics," *Science*, vol. 349, no. 6249, pp. 711–716, 2015, DOI: [10.1126/science.aab3642](https://doi.org/10.1126/science.aab3642).
- [3] J. Huh, G. G. Guerreschi, B. Peropadre, J. R. McClean, and A. Aspuru-Guzik, "Boson sampling for molecular vibronic spectra," *Nature Photonics*, vol. 9, no. 9, Art. no. 9, 2015, DOI: [10.1038/nphoton.2015.153](https://doi.org/10.1038/nphoton.2015.153).
- [4] A. Ribeiro and W. Bogaerts, "Digitally controlled multiplexed silicon photonics phase shifter using heaters with integrated diodes," *Optics Express*, vol. 25, no. 24, pp. 29778–29787, 2017, DOI: [10.1364/OE.25.029778](https://doi.org/10.1364/OE.25.029778).
- [5] A. Ribeiro, S. Declercq, U. Khan, M. Wang, L. V. Iseghem, and W. Bogaerts, "Column-Row Addressing of Thermo-Optic Phase Shifters for Controlling Large Silicon Photonic Circuits," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 26, no. 5, pp. 1–8, 2020, DOI: [10.1109/JSTQE.2020.2975669](https://doi.org/10.1109/JSTQE.2020.2975669).
- [6] H. Tang, S. Ohno, Y. Miyatake, K. Toprasertpong, S. Takagi, and M. Takenaka, "Thermo-optic Mach-Zehnder Interferometer Integrated with Si PN Diode Switch for Bipolar Optical Phase Control," in *Optical Fiber Communication Conference (OFC) 2021 (2021)*, paper Tu5B.5, Jun. 2021, p. Tu5B.5. DOI: [10.1364/OFC.2021.Tu5B.5](https://doi.org/10.1364/OFC.2021.Tu5B.5).
- [7] J.-H. Han, F. Boeuf, J. Fujikata, S. Takahashi, S. Takagi, and M. Takenaka, "Efficient low-loss InGaAsP/Si hybrid MOS optical modulator," *Nature Photonics*, vol. 11, no. 8, pp. 486–490, 2017, DOI: [10.1038/nphoton.2017.122](https://doi.org/10.1038/nphoton.2017.122).
- [8] M. Takenaka, J. Han, F. Boeuf, J. Park, Q. Li, C. P. Ho, D. Lyu, S. Ohno, J. Fujikata, S. Takahashi, and S. Takagi, "III-V/Si Hybrid MOS Optical Phase Shifter for Si Photonic Integrated Circuits," *Journal of Lightwave Technology*, pp. 1–1, 2019, DOI: [10.1109/JLT.2019.2892752](https://doi.org/10.1109/JLT.2019.2892752).
- [9] Q. Li, J.-H. Han, C. P. Ho, S. Takagi, and M. Takenaka, "Ultra-power-efficient 2 × 2 Si Mach-Zehnder interferometer optical switch based on III-V/Si hybrid MOS phase shifter," *Optics Express*, vol. 26, no. 26, p. 35003, 2018, DOI: [10.1364/OE.26.035003](https://doi.org/10.1364/OE.26.035003).