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Silicon MOS-capacitor modulators: scaling the modulation bandwidth, phase efficiency and compactness

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Abstract *We report silicon lateral MOS-capacitor modulators integrated within different thickness SOI wafers. The MZI modulators with lumped 2-segment electrodes are flip-chip bonded with CMOS drivers showing capability of 50 Gbaud PAM-4 transmission with 4 dB extinction ratio, 1.74 dB TDECQ and 2.4 pJ/bit power consumption. ©2022 The Author(s)*

Introduction

The continuous development of integrated silicon electro-optic modulators paves a practical solution to meet optical communication and computation bandwidths, and shows many benefits such as low cost, CMOS compatibility, high yield and mass volume production, which are vital for data infrastructures with Tb/s-scale inter-rack and intra-rack interconnects [1]–[4]. Recent developments of silicon photonic modulators have been dedicated towards tackling high modulation efficiencies, high bandwidth, and low driver voltages challenges by optimizing the plasma dispersion effect in p-n junctions built within Si waveguides. By applying a forward or reverse bias, current injection and depletion mechanisms can be utilized to modulate light up to several tens of Gb/s [5]–[8]. Typical depletion type modulators can operate with a 3 dB EO bandwidth around 35 GHz at a modulation efficiency $V_\pi L$, defined as the product of length (L) and voltage for full π phase change (V_π), of 1.6 Vcm [10][11] allowing 100 Gbaud communication with signal processing [7], [10].

Si–insulator–Si MOS-capacitor (MOSCAP) modulators working in the carrier accumulation regime have shown modulation efficiencies down to 0.3 Vcm and a data rate of 40 Gb/s [6]. The trade-off between high data rate and modulation efficiency can be controlled by changing the insulator equivalent oxide thickness (EOT). The highest speed to date of 60 Gb/s was achieved alongside an efficiency of 1.8 Vcm from a MOSCAP device incorporating polysilicon with lower carrier mobilities than that of single crystalline silicon [12]. In that case the bandwidth was close to that achieved in depletion modulators, but the insertion losses were high due to the polysilicon material used.

For other semiconductor solutions, n-type III-V/Si MOSCAP modulators were proposed to achieve the highest modulation efficiency with an excellent voltage and length product ($V_\pi L$,) as low as 0.047 Vcm [13] by taking advantage of the material's high electron mobility, low carrier-plasma absorption and large electron-induced refractive-index change. However, the RC bandwidth is limited to less than 1 GHz largely due to challenges in the fabrication process. A compromise of the modulation efficiency to a $V_\pi L$ of 0.37 Vcm was required to reach a data rate of 12.5 Gb/s [14]. To date, the highest data rate for a III-V/silicon hybrid MOS modulator is approximately 25 Gb/s [15], [16], where high-speed operation is achieved by drastically reducing the modulation efficiency to a relatively inefficient $V_\pi L$ of 1.3 Vcm [16] which allowed for a reduced loaded capacitance. In terms of the bandwidth, hybrid III-V/silicon modulators are so far inferior to all silicon MOSCAP modulators [6]. Hence, the trade-off between modulation bandwidth and efficiency for III-V/Si structures has led to a change of focus to other physical mechanisms such as the introduction of the Franz-Keldysh effect and carrier depletion effect in the reverse bias regime [17]. The RC bandwidth is then estimated to be above 100 GHz benefiting from a small depletion capacitance. It can be seen that achieving a high efficiency in combination with a high bandwidth in the carrier accumulation regime is very challenging, which makes it difficult to scale MZI modulators to sub-mm dimensions.

Here we demonstrate laterally stacked polysilicon/SiO_2/Si MOSCAP waveguide phase shifters with sub-10nm oxides in 8-inch SOI wafers with silicon overlayers of 520 nm and 220 nm, the phase efficiency of which can reach 0.35 Vcm and 0.65 Vcm, respectively. Benefiting from the high phase efficiency and its scalability, the MOSCAP phase shifter can be driven directly with lumped electrodes with segment lengths

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below 1mm. We here report an example of 100 Gb/s PAM-4 signal generation using our fabricated MOSCAP MZI modulators, which have two segments (of lengths 200μm and 400μm) driven by a co-designed and flip-chip bonded 28nm CMOS driver. The transmitter shows PAM-4 operation performance with a TDECQ of 1.74 dB and modulated extinction ratio (ER) 4 dB at the cost of 7 dB of optical loss.

Lateral MOSCAP modulators

Previously, we have fabricated lateral MOSCAP phase shifters using SOI wafer with a 320 nm silicon overlayer [18] and central SiO_2 insulator thickness of 10s of nanometers, resulting in phase change efficiencies of 1.8 Vcm, which is close to the efficiency of traditional depletion type PN-junction phase shifters. In order to scale the modulation size down to the sub-mm regime, here we fabricated 220 nm and 520 nm overlayer SOI based lateral MOSCAP waveguide phase shifters, which use polysilicon material on one side of the barrier realized by the fabrication method shown in [19]. The studied optical modes of the waveguide cross-sections are TM polarised for the 320 nm and 520 nm thick waveguides and TE polarised for the 220 nm thick waveguide. The schematic cross-sections of these MOSCAP waveguides are shown in Fig.1.

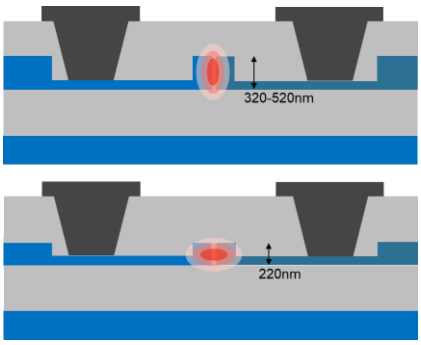

Fig.1 Schematic of the MOSCAP phase shifter cross-sections with silicon overlayers of 520 nm and 220nm, respectively.

The fabricated MZI modulators are first characterized with a forward bias voltage scan to extract the phase change efficiencies as shown in Fig.2. Thanks to the well-controlled central oxide thicknesses, which are approximately 5nm, the measured phase efficiency can reach 0.35 Vcm and 0.65 Vcm for 520 nm and 220 nm SOI based lateral MOSCAP waveguide phase shifters, respectively. The optical propagation losses are optimized to be 3-4 dB/mm for both cases. These high phase change efficiencies allow the MZI modulators to be directly driven by lumped electrodes with short phase shifter segments (<1mm length), which will be discussed and demonstrated with and without CMOS drivers in later sections.

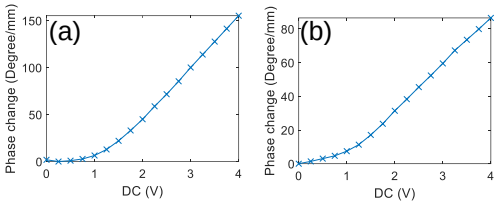

Fig.2. Experimentally measured phase change versus applied forward bias voltage for the MOSCAP phase shifter with 520nm (a) and 220nm (b) Si overlayer thicknesses.

Segmented MOSCAP MZI modulator

Experimentally, the MZI modulators with two different length phase shifter segments (300μm and 600μm) are tested using 50-ohm terminated GSGSG probes with a 3 Vpp differential RF signal applied and a DC bias voltage close to 1 V. The two segments can support 50 Gb/s OOK operation when biased at 0.7 V as shown in Fig.3. The eye quality is limited due to impedance matching with the conventional 50-ohm RF testing equipment and the total capacitance that the lumped model can support due to the 50-ohm RF source impedance. With 3-tap FFE, the obtained eye diagrams are clear and open as displayed in Fig.3.

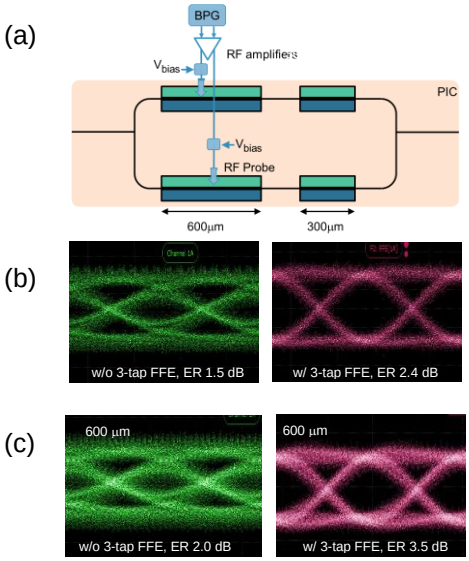

Fig.3 High speed testing of segmented silicon MOSCAP MZI modulators using external Bit-Pattern-Generator, RF amplifier, bias-Tee and RF probes to driver the signal to the lumped MOSCAP segment (a). The measured optical eye diagrams w/o and w/ 3-taps FFE at 50 Gb/s for segment lengths of 300μm (b) and 600μm (c).

CMOS driver integration with MOSCAP modulators

One of the benefits of using MOSCAP phase shifters for MZI modulators is that the lengths of

the phase shifters can be scaled down to their optimum compactness, which would exhibit a reasonable capacitance level, for which CMOS drivers can be specifically co-designed with pre-emphasis techniques to extend the EO bandwidth and minimize the power consumption. As discussed in the previous section, a segment length of 600 μm leads to a high capacitance close to 1 pF when driven completely in accumulation mode. The CMOS drivers should drive less capacitance when the MOSCAP junction is biased lower than 2V, which makes it more practical to achieve high performance 50 Gbaud PAM-4 operation in such scenarios.

Here we show that the MOSCAP modulators can demonstrate much better performance when driven with a custom co-designed 28nm CMOS driver with built-in controllable pre-distortion and inductive peaking techniques to achieve better bandwidth and power consumption [20], as schematically shown in Fig.4. Two-channel drivers are flip-chip bonded with the segmented MOSCAP modulator chips. The packaged transmitter shows PAM-4 operation performance with a TDECQ of 1.74 dB and ER of 4 dB as shown in Fig.4(b). The optical loss is around 7 dB and the power consumption is approximately 2.4 pJ/bit [20].

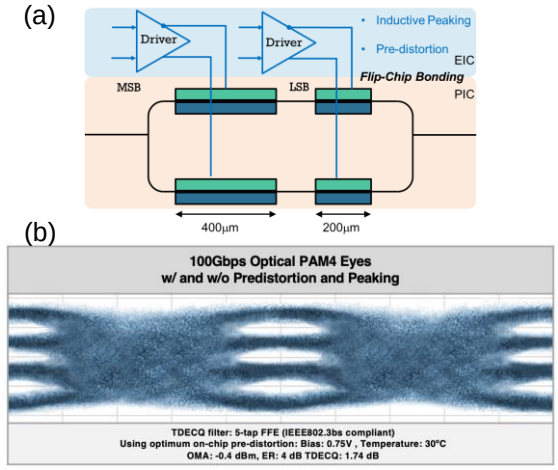

Fig.4. (a) Schematic of the CMOS drivers flipped-bonded with MOSCAP modulators for PAM-4 operation. (b) Obtained PAM-4 eye diagram with TDECQ filter (5-tap FFE), showing modulated ER 4 dB and TDECQ 1.7 dB when the MOSCAP junction is biased at 0.75 V.

Conclusions

We report on lateral MOSCAP modulators fabricated in SOI wafers with Si overlayer thicknesses of 220nm and 520nm. Their modulation efficiencies reach 0.65 Vcm to 0.35 Vcm, respectively, showing the capability to scale the MZI modulators with compactness below 1 mm together with a bandwidth for 50Gbaud PAM-4 operation. The packaged MOSCAP transmitter, with built-in pre-distortion and inductive peaking techniques in a co-designed 28nm CMOS driver, has demonstrated PAM-4 operation with a TDECQ of 1.74 dB, modulated ER of 4 dB, optical loss of around 7 dB and power consumption at approximately 2.4 pJ/bit.

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