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1×40 100 GHz spacing Low-crosstalk Mux/Demux based on Cascaded Planar Echelle Gratings on 3-μm Silicon platform

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Abstract *We experimentally demonstrate a photonic integrated 1×40 100GHz spaced Mux/Demux by cascading one 1×8 100GHz 3-μm silicon Planar Echelle Grating (PEG) and eight 1×5 800GHz PEGs. Experimental results show 2dB insertion loss, -35dB crosstalk and error-free operation at 10Gb/s with <0.1dB power penalty. © 2022 The Author(s)*

Introduction

Wavelength Division Multiplexing (WDM) systems employing photonic integrated wavelength multiplexers and demultiplexers (Mux/Demux) are effectively used to increase the data capacity of the optical fiber transmission as well as transparently route the wavelength channels in advanced data center and metro-access network [1,2]. Arrayed waveguide gratings (AWG) in silica are commercially available [3]. However, in photonic integrated circuits based on different technologies such as SiPh or InP, when the required channel number increases > 16 and channel spacing decreases <100GHz, the AWG's performance (insertion loss and crosstalk) will drop due to increased arrayed waveguide number and chip size [3]. Compared with the AWG, the PEG offers a better solution for large channel WDM system due to the smaller size by reusing the free propagation region (FPR) for wavelength injection and diffraction. Also, the PEG has relatively larger Rowland circle (RC) than AWG for placing more output ports.

Several PEGs were fabricated on different integrated photonic platforms: the 30-channels PEG based on 220-nm silicon on insulator (SOI) platform with 400 GHz spacing has an insertion loss between 3 dB to 7 dB and high crosstalk from -15 dB to -25 dB [4]. In [5] it has been demonstrated 48-channels 100 GHz spaced silica PEG with -35 dB crosstalk, but with very large size of 306 (18×17) mm^2.

In this paper, we experimentally demonstrate for the first time a compact (25 mm^2) 40-channels 100 GHz spacing low-crosstalk (-35 dB) Mux/Demux using cascaded PEGs on 3-μm silicon platform. To effectively reduce the crosstalk of the PEG with narrow channel spacing and large output port number, we employ the cascaded two stage PEGs: the 1st stage is one conventional 1×8 cyclic PEG with 100 GHz spacing, and 2nd stage uses eight 1×5 800 GHz spaced PEGs, whose inputs connect the output ports of 1×8 cyclic PEG, respectively (see the configuration in Fig. 1 (a)). The crosstalk is decreased effectively by the two-stages filtering. Also, to avoid accumulated crosstalk caused by fabrication error and reduce chip size, the ultra-low loss 3-μm SOI platform is employed for realizing the cascaded design. The insertion losses of all 40 channels range from 2 dB to 5 dB with ~100 GHz spacing. And by re-using of the

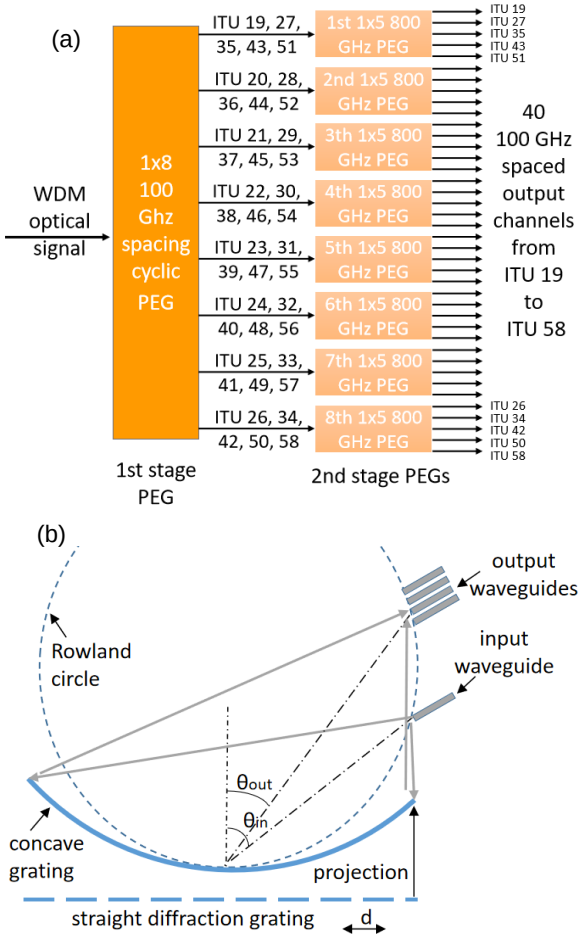

Fig. 1: (a) the schematic of the 1×40 100 GHz Mux/Demux using the cascaded one 1×8 100 GHz PEG and eight 1×5 800 GHz PEGs; (b) the structure of the Rowland type PEG.

FPR, the 1×40 100 GHz PEG has compact size of only 25 mm^2. The data transmission experiment shows error free operation with < 0.1 dB power penalty at 10 Gb/s NRZ-OOK signal.

Operation of the 1×40 100 GHz spacing Mux/Demux

The operation schematic of the 1x40 100GHz spacing Mux/ Demux by cascading two stage PEGs is shown in Fig 1 (a). The 1st stage PEG is cyclic and has 8 output ports with 100 GHz spacing, and 2nd stage employs eight 1×5 800 GHz spaced PEGs, whose inputs connect the output ports of 1×8 cyclic PEG, respectively. The design and operation of the two Rowland type PEGs are based on the structure shown in Fig. 1 (b). The input and output waveguides of the PEG are placed on the RC. The concaved grating with reflective coating is the projection of the conventional straight grating. The incident WDM channels are diffracted and focused on the RC, so that the different wavelengths are separated to different output ports. More detailed working principle of the PEG is described is [6]. And EPIPPROP is employed for design of the photonic integrated circuit.

The primary cyclic 1x8 PEG (1st stage) is designed with 8 output waveguides, 100 GHz channel spacing, and 6.4 nm (800 GHz) free spectral range (FSR) for achieving cyclic operation. The central wavelengths of each of the eight outputs are set to match the ITU DWDM grid, from 1st channel (ITU 19: 1562.23 nm) to 8th channel (ITU 26: 1556.55 nm) with 100 GHz (0.8 nm) channel spacing. Therefore, the first output of the primary PEG selects five channels in the C-band: 1562.23 nm (191.9 THz), 1555.75 nm (191.9 THz + 0.8 THz), 1549.32 nm (191.9 THz + 2*0.8 THz), 1542.94 nm (191.9 THz + 3*0.8 THz), 1536.61 nm (191.9 THz + 4*0.8 THz) (see Fig. 1 (a)). The second output of the primary PEG will select other 5 channels from ITU 20 (1561.42 nm) to ITU 52: 1535.82 nm with steps of 800 GHz (see Fig. 1 (a)). Same for the other outputs of the primary PEG, each of them selects 5 wavelengths. To achieve 40 individual output channels, every output of the primary PEG is connected (input) to one 1×5 800 GHz spaced PEG with different central wavelength (100 GHz shift). Each 2nd stage PEG provides 5 outputs with 800 GHz spacing to match the FSR of primary PEG as well as the central wavelength. With eight different 1×5 800 GHz spaced PEGs, the cascaded PEG can select 40 output channels totally. Note that due to the double filtering, the crosstalk can be effectively reduced.

Fabrication of the PEG

VTT 3-µm SOI platform with wide-band single mode waveguide and ultra-dense integration [7] is used for realizing the cascaded PEG with low loss and crosstalk. The micrograph of the fabricated cascaded PEG is shown in Fig. 2. As briefly mentioned earlier, the chip is fabricated as part of a multi-project wafer (MPW) run based on the VTT 3-µm SOI photonic integrated platform [7] on enhanced silicon-on-insulator (ESOI, 3-µm top Si on 3-µm buried oxide) wafers from Okmetic. Fabrication technology is based on an i-line stepper on the 150-mm wafer size, and a double-step Si etching process with SiO_2 hard-mask is implemented to form the rib-strip waveguide structure [8]. Wet thermal oxide growth and removal with buffered oxide etch (BOE) is used for smoothening the etched Si surfaces [9]. Input/output waveguides and grating facets are etched separately on the wafer. The latter is sputtered with 250-nm reflector aluminum, and a 265-nm thick SiO_2 layer works as a quarter-wave to improve the reflectivity of the aluminum layer from 92% to 98% [9]. Single layer silicon nitride is deposited on input/output waveguide facets as antireflection coating to reduce the coupling loss between waveguides and fibers. The chip is protected with a 500 nm cladding SiO_2 deposition.

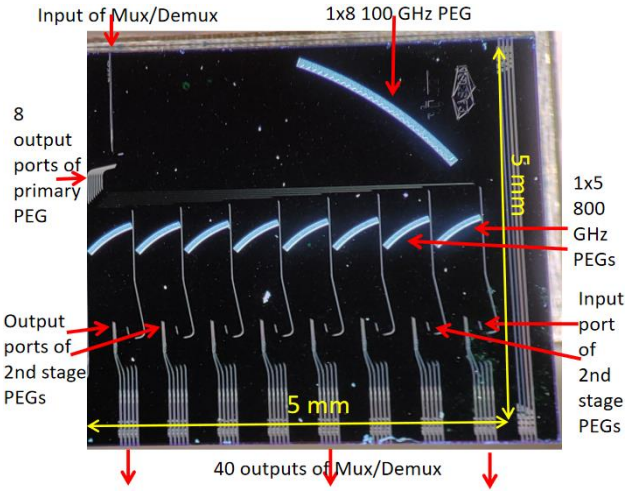

Fig. 2: The micrograph of the fabricated cascaded 1×40 100 GHz PEG.

Experimental results

Fig. 3 shows the experimental setup for the chip characterization. Firstly, we characterize the 40 output channels transfer function by using a tunable laser covering the C-band, a polarization controller, a polarization analyzer, lensed fibers to couple the light into the chip and an optical spectrum analyser (OSA) for recording the spectrum. Fig. 4 shows the experimental transmission spectrum of the fabricated 1×40 100

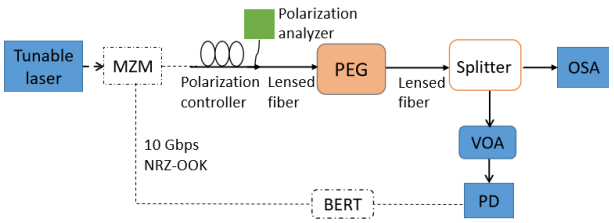

Fig. 3: The experimental set-up.

To quantify the possible signal degradation from the PEG, BER curves are measured for five different channels spanning the C-band (1559.79 nm, 1553.33 nm, 1546.92 nm, 1540.56 nm and 1534.25 nm) for TE mode with 10Gb/s NRZ-OOK 2^{31}-1 PRBS signal. In the BER measurements, a 10Gb/s Mach-Zehnder Modulator (MZM) is used to generate the data signal. The BER curves are

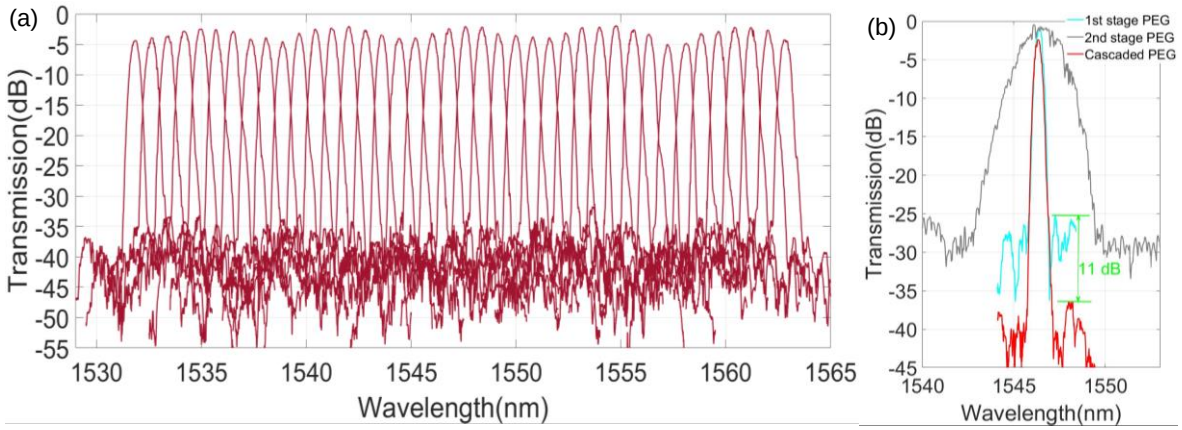

Fig. 4: (a) 40 channels output spectrum of the cascaded PEG for TE mode, (b) overlapped spectrum of 1st stage PEG, 2nd stage PEG and cascaded PEG.

GHz device for TE mode. The lowest insertion loss of 2 dB was measured (after removing the coupling losses of 2 dB per facet). The highest insertion loss for the worse channel is around 5 dB. The loss variations of all 40 channels are < 3 dB and caused by the small FSR. The noise floor (causing crosstalk for other channels) is reduced with 11 dB improvement by cascaded connection (see Fig. 4 (b), the spectrum was measured with independent 1st and 2nd stage PEGs chips without cascaded connection). The measured crosstalk levels are between -30 dB and -35 dB. The measured channel spacing is ~0.8 nm (~100 GHz) in average and matches the design. And the channel wavelength shift comparing with ITU DWDM grid is less than 0.1 nm and may be caused by the wafer's thickness variation.

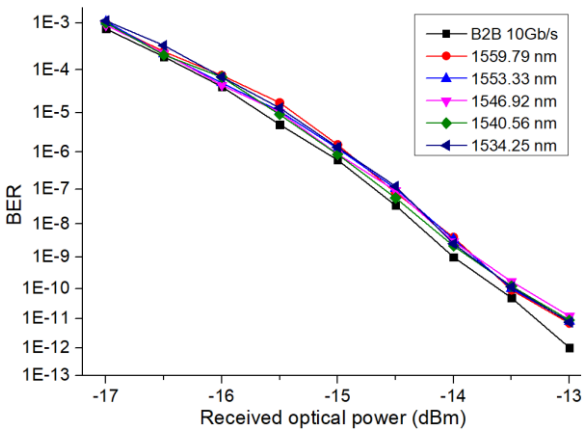

Fig. 5: BER curves of five wavelengths at 10 Gb/s.

illustrated in Fig. 5. The back-to-back (B-to-B) BER curve is also reported as reference. It shows that error-free operation for all five channels after the Mux/Demux are observed with power penalty less than 0.1 dB at BER of 1E-9. The result shows the very limited impact of the cascaded PEG on the modulated optical signals.

Conclusions

We have demonstrated a novel photonic integrated 40-channels 100 GHz spaced Mux/Demux based on the cascaded one 1×8 100 GHz PEG and eight 1×5 800 GHz PEGs designed and fabricated on 3-µm SOI platform. Experimental results show the insertion losses ranging from 2 dB to 5 dB, low crosstalk levels (-30 dB to -35 dB) and ~ 100 GHz channel spacing for all 40 channels. The size of the fabricated 1×40 PEG is only 25 mm^2. BER measurements on five representative channels spanning the C-band at 10 Gb/s NRZ-OOK data signal confirm the error-free operations with power penalty < 0.1 dB at BER of 10E-9.

Acknowledgements

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