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DFE State-Tracking Demapper for Soft-Input FEC in 800G Data Center Interconnects

Kaiquan Wu, Gabriele Liga, Jeffrey Lee, Lotte Paulissen, Jamal Riani*, and Alex Alvarado

Eindhoven University of Technology, 5600MB Eindhoven, The Netherlands k.wu@tue.nl
*Marvell Technology, Santa Clara, CA, USA

Abstract *A simple one-step state model is used to track the DFE error propagation for 4-PAM. The knowledge of DFE output states is used to improve LLR accuracy. Demapping via DFE state tracking outperforms bit-interleaving and precoding schemes for the 802.3ca LDPC code by* 0.76 *dB.*

Introduction

Data center interconnects are currently undergoing a transition from 400Gb/s to 800Gb/s. As intensity modulation (IM) and direct detection (DD) scheme has been widely employed in transceivers, advanced coded modulation (CM) schemes that can accommodate such high speeds and also meet low complexity, low-cost and low-latency requirements[1] are desirable. 4-ary pulse amplitude modulation (PAM) is a crucial element in these CM schemes due to its good spectral efficiency delivered with simple direct detection[2]. Another important element is forward error correction (FEC), which is a key enabler to maximize link budget and relaxing component specifications. Despite relative high power consumption, powerful soft-input FEC such as low-density parity-check (LDPC) codes appear to be a more appealing choice than hard-input FEC.

The high data rates imply worse inter-symbol interference (ISI). This can be resulted from IMDD optical links, or bandlimited components from existing interconnects. Currently, simple equalization schemes like feedforward equalization (FFE) and decision-feedback equalizers (DFE) can cancel ISI. However, DFE causes error propagation, leading to residual distortions in the equalized signal. The DFE error propagation is harmful to FEC decoding. When hard-input FEC is used, the decoding is negatively affected by the frequent appearance of consecutive errors per codeword[3]. As for soft-input FEC, error propagation affects the log-likelihood ratio (LLR) distribution which strongly impairs the decoding performance[4].

In the presence of DFE, mismatched LLRs are calculated by assuming only additive white Gaussian noise (AWGN) imposed on the equalized symbols. More sophisticated approaches such as the Bahl-Cocke-Jelinek-Raviv algorithm[5] or the soft-output Viterbi algorithm[6],[7] can be used for accurate LLR output but at the cost of high complexity. Alternatively, the detrimental impact of error propagation can be alleviated by using bit-interleaving or precoding, as done, for instance, in the IEEE 802.3ca standard[8]. However both these techniques have drawbacks: interleaving increases latency and cannot cope with mismatched LLRs[4], whilst typically no soft-output is available with a precoding scheme. In fact, the impact of DFE error propagation can be analyzed by using a finite-state transition model describing the evolution of the decision errors. To evaluate bit error rate (BER) of FEC, several finite-state transition models have been proposed[3],[9]–[11].

In this paper, a scheme is proposed to improve the LLR calculation for DFE-equalized channels. The proposed scheme consists of two stages. First, a one-step state transition model within DFE tracks the state probabilities recursively. Second, the state probabilities are used in the LLR calculation. The proposed scheme outperforms both interleaving or precoding with mismatched LLRs in terms of post-FEC BER performance.

4PAM DFE State Tracking

In this paper, we consider a partial response (PR) channel with two-tap impulse response $[1, \alpha]$ as shown in Fig. 1, which is also considered in[4]. At time instant i, the received symbol is given by

$$y_i = x_i + \alpha x_{i-1} + n_i, \tag{1}$$

where n_i stands for the AWGN with noise variance σ^2, and $x_i \in \mathcal{X} = \{\pm 1, \pm 3\}$ (4-PAM). The minimum euclidean distance of $\mathcal{X}$ is $d = 2$.

DFE cancels the ISI in y_i by exploiting the previous hard decision (HD) $\hat{x}_{i-1}$, i.e.,

$$\overline{y}_i = y_i - \alpha \hat{x}_{i-1}, \tag{2}$$

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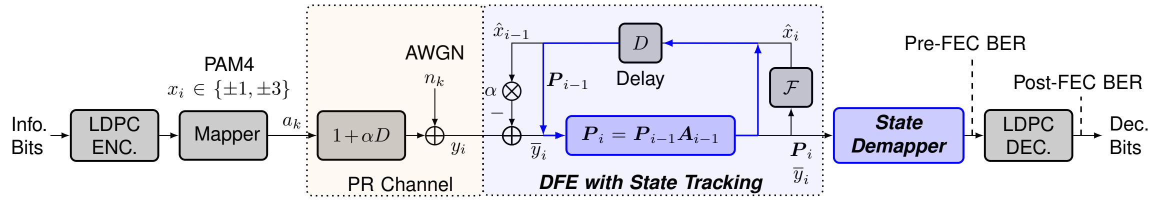

Fig. 1: Block diagram of PR channel transmission setup using state-tracking DFE and state demapper.

where $\hat{x}_{i-1}$ is obtained by comparing $\overline{y}_{i-1}$ using a three-level slicer $\{0, \pm d\}$. This decision operation is denoted as $\hat{x}_{i-1} = \mathcal{F}(\overline{y}_{i-1})$.

The error produced by DFE is $e_i = x_i - \hat{x}_i$, where $e_i \in \{0, \pm d, \pm 2d, \pm 3d\}$. After the DFE feedback (shown as a black loop in Fig. 1), e_i lead to different biased states for $\overline{y}_i$, which from (2) gives $\overline{y}_i = x_i + n_i + \alpha e_{i-1}$. For high signal-to-noise ratios (SNRs), the majority of errors occur between neighbouring symbols. Hence, the reduced set $e_{i-1} \in \mathcal{S} = \{-d, 0, d\}$ is considered in this paper. The resultant state is represented as $s_i \in \{l, c, r\}$, which stand for left-biased, center, and right-biased states, respectively.

The state probabilities conditioned on the previous equalized symbol are of our interests, and thus a vector $\boldsymbol{P}_i$ is defined as

$$\boldsymbol{P}_i = \left[P(s_i|\overline{y}_{i-1}, \overline{y}_{i-2}, \ldots)\right], s_i = l, c, r. \quad (3)$$

The summation of $\boldsymbol{P}_i$ elements is 1. We assume $x_0 = 0$, and thus the first transmitted symbol x_1 does not experience ISI and $\boldsymbol{P}_1 = [0, 1, 0]$.

To track the evolution of the DFE states, we propose to use a finite-state machine as shown in Fig. 2. The nodes and edges indicate the states and their transitions. The state transition probability is defined as $P_{S|S} \triangleq P(s_i|\overline{y}_{i-1}, s_{i-1})$, which depends on the observation of $\overline{y}_{i-1}$ and s_{i-1}. Two major loops in Fig. 2 characterize the DFE behaviour. The blue loop indicates an error-free output, where the state stays at c. The error propagation is captured by the red loop between l and r. In this loop, DFE will make decisions with a bias $\pm\alpha d$, and becomes more susceptible to an error. If the error propagation continues, the next state will be directed to the opposite side, forcing errors d and $-d$ occur in turn.

Based on the state transition model, $\boldsymbol{P}_i$ then can be inferred recursively, i.e.,

$$\boldsymbol{P}_i = \boldsymbol{P}_{i-1}\boldsymbol{A}_{i-1}, \quad (4)$$

where $\boldsymbol{A}_{i-1}$ is a matrix of $P_{S|S}$. Compared to standard DFE, state tracking only requires a recursive operation, as emphasized in blue in Fig. 1.

The key to the recursive inference is $\boldsymbol{A}_{i-1}$. We

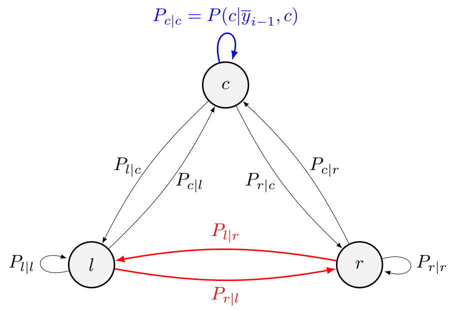

Fig. 2: DFE state transition model. Error propagation is highlighted with red and error-free output with blue.

start by considering an intermediate matrix $\boldsymbol{B}_{i-1}$. By defining an offset ϕ, we assume a Gaussian distribution $\overline{y}_{i-1} \sim \mathcal{N}(\hat{x}_{i-1} + \phi, \sigma^2)$, and its probability density function (PDF) is denoted as $\varphi(\phi)$. When $\hat{x}_{i-1} = \pm 1$, $\boldsymbol{B}_{i-1}$ is given by

$$\boldsymbol{B}_{i-1} = \begin{bmatrix} \varphi(d+\alpha d) & \varphi(\alpha d) & \varphi(-d+\alpha d) \\ \varphi(d) & \varphi(0) & \varphi(-d) \\ \varphi(d-\alpha d) & \varphi(-\alpha d) & \varphi(-d-\alpha d) \end{bmatrix}. \quad (5)$$

When $\hat{x}_{i-1}$ is the outermost symbol, as there is no neighbouring symbol on either side, the error can only lead to one biased state. Therefore, when $\hat{x}_{i-1} = -3$ or 3, the left or right column of $\boldsymbol{B}_{i-1}$ in (5) is set to a zero column vector. Finally, $\boldsymbol{A}_{i-1}$ is obtained by doing a row normalization on $\boldsymbol{B}_{i-1}$.

State Demapper

A typical soft demapper after DFE implicitly assumes the DFE is constantly in state c (correct decision on the previous symbol). After dropping the time index i, the resulting mismatched LLR is then given by

$$L_k = \log \frac{\sum_{x \in \mathcal{X}_k^1} f_{\overline{Y}|X}(\overline{y}|x)}{\sum_{x \in \mathcal{X}_k^0} f_{\overline{Y}|X}(\overline{y}|x)}, \quad (6)$$

where $k = 1, 2$, and $\mathcal{X}_k^b \subset \mathcal{X}$ are 4-PAM symbols labeled by a bit $b \in \{0, 1\}$ at position k. $f_{\overline{Y}|X}(\overline{y}|x)$ is the PDF given by the distribution $\overline{y} \sim \mathcal{N}(x, \sigma^2)$.

The state demapper takes advantage of the different state probabilities inferred by the state-tracking DFE and computes the LLR at time i as

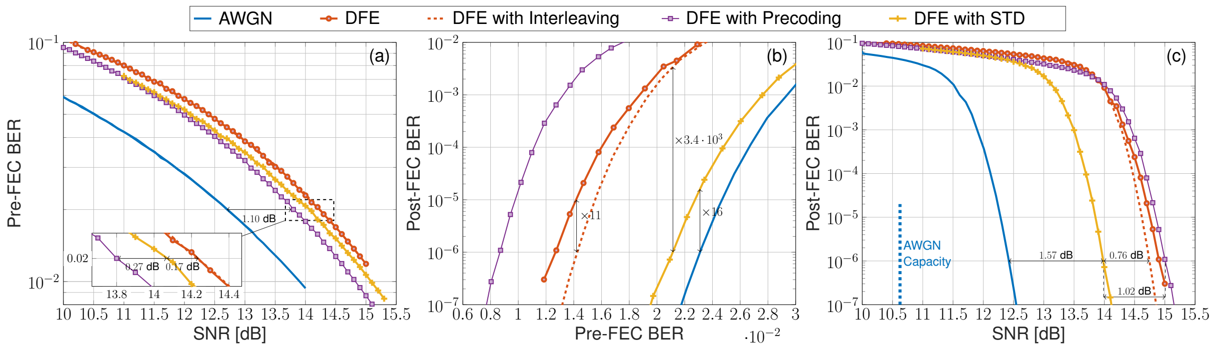

Fig. 3: (a) Pre-FEC BER vs. SNR; (b) Pre-FEC BER vs. Post-FEC BER; (c) Post-FEC BER vs. SNR.

$$L_k^{\mathbf{S}} = \log \frac{\sum_{x\in\mathcal{X}_k^1} \sum_{s\in\mathcal{S}} f_{\overline{Y}|X,S}(\overline{y}|x,s)P(s|\overline{\boldsymbol{y}}')}{\sum_{x\in\mathcal{X}_k^0} \sum_{s\in\mathcal{S}} f_{\overline{Y}|X,S}(\overline{y}|x,s)P(s|\overline{\boldsymbol{y}}')}, \tag{7}$$

where $\overline{\boldsymbol{y}}' = [\overline{y}_0, \overline{y}_1, ..., \overline{y}_{i-1}]$ denotes the vector of past equalized symbols. In (7), $f_{\overline{Y}|X,S}(\overline{y}|x,s)$ is given by $\overline{y} \sim \mathcal{N}(x+\phi, \sigma^2)$, where $\phi = -\alpha d, 0, \alpha d$ for states l, c, and r, respectively.

Numerical Results

In this section, we numerically evaluate the performance of the state-tracking DFE together with state demapper, which is referred as STD. The system under consideration is the one depicted in Fig. 1, where $\alpha = 0.6$. Other schemes are also shown for comparison, including DFE, DFE with bit-interleaving (random interleaving across 4 codewords), and DFE with precoding. In addition, performance in the AWGN channel (ISI-free) is shown as a reference. The IEEE 802.3ca standard LDPC code is used with blocklength of 17664 bits and code rate 0.83. The decoder receives LLRs and performs belief propagation (BP) with 6 iterations. For precoding scheme, the demapper transforms each HD into a fixed LLR[12]. For unitary signal power, the SNR is defined as $1/\sigma^2$.

We investigate the performance in three aspects: i) equalization; ii) improved demapping; iii) combined equalization, demapping, and decoding performance. The equalization effectiveness is shown in Fig. 3(a), where the pre-FEC BER vs. SNR is plotted. In the case of DFE with STD, pre-FEC BER is computed by making hard decisions on the LLRs in (7). For other schemes, bits are obtained by demapping hard decision symbols into bits. A gap over 1.1 dB is observed between the AWGN and the PR channel using DFE. Since interleaving has no effect on reducing pre-FEC BER, DFE with or without interleaving show the same equalizing ability. At a BER of 0.02, STD gains 0.17 dB for DFE due to the improved LLR accuracy. Precoding appears to be the most effective strategy to reduce pre-FEC errors, which gives an extra gain of 0.27 dB with respect to STD.

Fig. 3(b) shows post-FEC BER vs. pre-FEC BER. For soft-input FEC, the decoding ability largely depends on the LLR accuracy. When precoding is used, because the soft information of de-precoded symbols is not available, quantized LLRs are used and thus a significant performance degradation is observed. By removing error correlations, DFE with interleaving reduces post-FEC BER by one order of magnitude compared to DFE. Compared using interleaving, STD can decrease the post-FEC BER by more than three orders of magnitude (3.4×10^{-3}), performing closer to the AWGN scenario ($\times 16$ lower BER).

Finally, post-FEC BER vs. SNR is shown in Fig. 3(c). In combination of DEF, STD significantly outperforms interleaving and precoding schemes. Compared to interleaving, STD gives an extra gain of 0.76 dB for DFE at a BER of 10^{-6}. Although DFE with precoding reduces pre-FEC BER, its post-FEC performance is the worst due to the LLR quantization. Finally, a gap of 1.57 dB between the DFE with STD scheme and the AWGN performance can be observed.

Conclusions

We proposed a state-tracking DFE which recursively infers the probability of biased states in partial response channels such as those relevant in high-speed PAM optical systems in data center interconnects. The state probabilities are then used in a state demapper to compute improved LLRs. Numerical results show that by computing more accurate LLRs, significant gains after LDPC decoding are achieved compared to standard DFE, and DFE with interleaving or precoding. The proposed scheme is an interesting option to improve the performance of soft-decision coded data center interconnects with limited increase in complexity. The complexity of our proposed scheme can be decreased further via a PDF lookup table. This is left for future investigation.

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